Agilent 75000 SERIES C

Model D20
Digital Functional Test System

Service Manual

The information in this manual applies to the following equipment.

Agilent E1450A Timing Modules
Agilent E1451A Pattern I/O Modules
Agilent E1452A Terminating Pattern I/O Modules
Agilent E1453A Timing Pods
Agilent E1454A Pattern I/O Pods
Agilent E1455A Timing Pods
Agilent E1456A Pattern I/O Pods

Agilent Technologies

E1450-90010

Manual Part Number: E1450-90010
Microfiche Part Number: E1450-99010

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Certification

Agilent Technologies certifies that this product met its published specifications at the time of shipment from the factory. Agilent Technologies further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by that organization's calibration facility, and to the calibration facilities of other International Standards Organization members.

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For warranty service or repair, this product must be returned to a service facility designated by Agilent Technologies. Buyer shall prepay shipping charges to Agilent and Agilent shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to Agilent from another country.

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Agilent E1450A through E1456A Model D20 Digital Functional Test System Service Manual
Edition 1 Rev 2

Printing History

The Printing History shown below lists all Editions and Updates of this manual and the printing date(s). The first printing of the manual is Edition 1. The Edition number increments by 1 whenever the manual is revised. Updates, which are issued between Editions, contain replacement pages to correct the current Edition of the manual. Updates are numbered sequentially starting with Update 1. When a new Edition is created, it contains all the Update information for the previous Edition. Each new Edition or Update also includes a revised copy of this printing history page. Many product updates or revisions do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

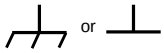
Edition 1 (Part Number E1450-90010). . . . . June 1992

Edition 1 Rev 2 (Part Number E1450-90010) . . . . . April 2006

Safety Symbols

Instruction manual symbol affixed to product. Indicates that the user must refer to the manual for specific WARNING or CAUTION information to avoid personal injury or damage to the product.

Indicates the field wiring terminal that must be connected to earth ground before operating the equipment—protects against electrical shock in case of fault.



Frame or chassis ground terminal—typically connects to the equipment's metal frame.

Alternating current (AC).

Direct current (DC).

Indicates hazardous voltages.

WARNING Calls attention to a procedure, practice, or condition that could cause bodily injury or death.

CAUTION Calls attention to a procedure, practice, or condition that could possibly cause damage to equipment or permanent loss of data.

WARNINGS

The following general safety precautions must be observed during all phases of operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the product. Agilent Technologies assumes no liability for the customer's failure to comply with these requirements.

Ground the equipment: For Safety Class 1 equipment (equipment having a protective earth terminal), an uninterruptible safety earth ground must be provided from the mains power source to the product input wiring terminals or supplied power cable.

DO NOT operate the product in an explosive atmosphere or in the presence of flammable gases or fumes.

For continued protection against fire, replace the line fuse(s) only with fuse(s) of the same voltage and current rating and type. DO NOT use repaired fuses or short-circuited fuse holders.

Keep away from live circuits: Operating personnel must not remove equipment covers or shields. Procedures involving the removal of covers or shields are for use by service-trained personnel only. Under certain conditions, dangerous voltages may exist even with the equipment switched off. To avoid dangerous electrical shock, DO NOT perform procedures involving cover or shield removal unless you are qualified to do so.

DO NOT operate damaged equipment: Whenever it is possible that the safety protection features built into this product have been impaired, either through physical damage, excessive moisture, or any other reason, REMOVE POWER and do not use the product until safe operation can be verified by service-trained personnel. If necessary, return the product to an Agilent Technologies Sales and Service Office for service and repair to ensure that safety features are maintained.

DO NOT service or adjust alone: Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT substitute parts or modify equipment: Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to an Agilent Technologies Sales and Service Office for service and repair to ensure that safety features are maintained.

DECLARATION OF CONFORMITY

According to ISO/IEC Guide 22 and CEN/CENELEC EN 45014

CE

Manufacturer's Name: Agilent Technologies, Incorporated
Manufacturer's Address: 815 – 14th St. SW
Loveland, Colorado 80537
USA

Declares, that the product

Product Name: 160 MHz Timing Module
Model Number: E1450A and associated timing pods E1453A and E1455A
Product Options: *This declaration covers all options of the above product(s).*

Conforms with the following European Directives:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly.

Conforms with the following product standards:

EMC	**Standard**	**Limit**
	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
	CISPR 11:1990 / EN 55011:1991	*Group 1 Class A*
	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995	*4kV CD, 8kV AD*
	IEC 61000-4-3:1995 / EN 61000-4-3:1995	*3 V/m, 80-1000 MHz*
	IEC 61000-4-4:1995 / EN 61000-4-4:1995	*0.5kV signal lines, 1kV power lines*
	IEC 61000-4-5:1995 / EN 61000-4-5:1995	*0.5 kV line-line, 1 kV line-ground*
	IEC 61000-4-6:1996 / EN 61000-4-6:1996	*3V, 0.15-80 MHz I cycle, 100%*
	IEC 61000-4-11:1994 / EN 61000-4-11:1994	*Dips: 30% 10ms; 60% 100ms* *Interrupt > 95%@5000ms*
	Canada: ICES-001:1998 *Australia/New Zealand: AS/NZS 2064.1*	
	The product was tested in a typical configuration with Agilent Technologies test systems.	
Safety	*IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995* *Canada: CSA C22.2 No. 1010.1:1992* *UL 3111-1: 1994*	

1 June 2001
Date

Ray Corson
Product Regulations Program Manager

For further information, please contact your local Agilent Technologies sales office, agent or distributor.
Authorized EU-representative: Agilent Technologies Deutschland GmbH, Herrenberger Strabe 130, D 71034 Böblingen, Germany

DECLARATION OF CONFORMITY

According to ISO/IEC Guide 22 and CEN/CENELEC EN 45014

Agilent Technologies

CE

Manufacturer's Name: Agilent Technologies, Incorporated
Manufacturer's Address: 815 – 14th St. SW
Loveland, Colorado 80537
USA

Declares, that the product

Product Name: 20 MHz Pattern I/O Module
Model Number: E1451A/E1452A and associated E1454A/E1456A Pattern I/O Pods
Product Options: *This declaration covers all options of the above product(s).*

Conforms with the following European Directives:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly.

Conforms with the following product standards:

EMC	**Standard**	**Limit**
	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
	CISPR 11:1990 / EN 55011:1991	*Group 1 Class A*
	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995	*4kV CD, 8kV AD*
	IEC 61000-4-3:1995 / EN 61000-4-3:1995	*3 V/m, 80-1000 MHz*
	IEC 61000-4-4:1995 / EN 61000-4-4:1995	*0.5kV signal lines, 1kV power lines*
	IEC 61000-4-5:1995 / EN 61000-4-5:1995	*0.5 kV line-line, 1 kV line-ground*
	IEC 61000-4-6:1996 / EN 61000-4-6:1996	*3V, 0.15-80 MHz I cycle, 100%*
	IEC 61000-4-11:1994 / EN 61000-4-11:1994	*Dips: 30% 10ms; 60% 100ms* *Interrupt > 95%@5000ms*
	Canada: ICES-001:1998 *Australia/New Zealand: AS/NZS 2064.1*	
	The product was tested in a typical configuration with Agilent Technologies test systems.	
Safety	*IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995* *Canada: CSA C22.2 No. 1010.1:1992* *UL 3111-1: 1994*	

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Date

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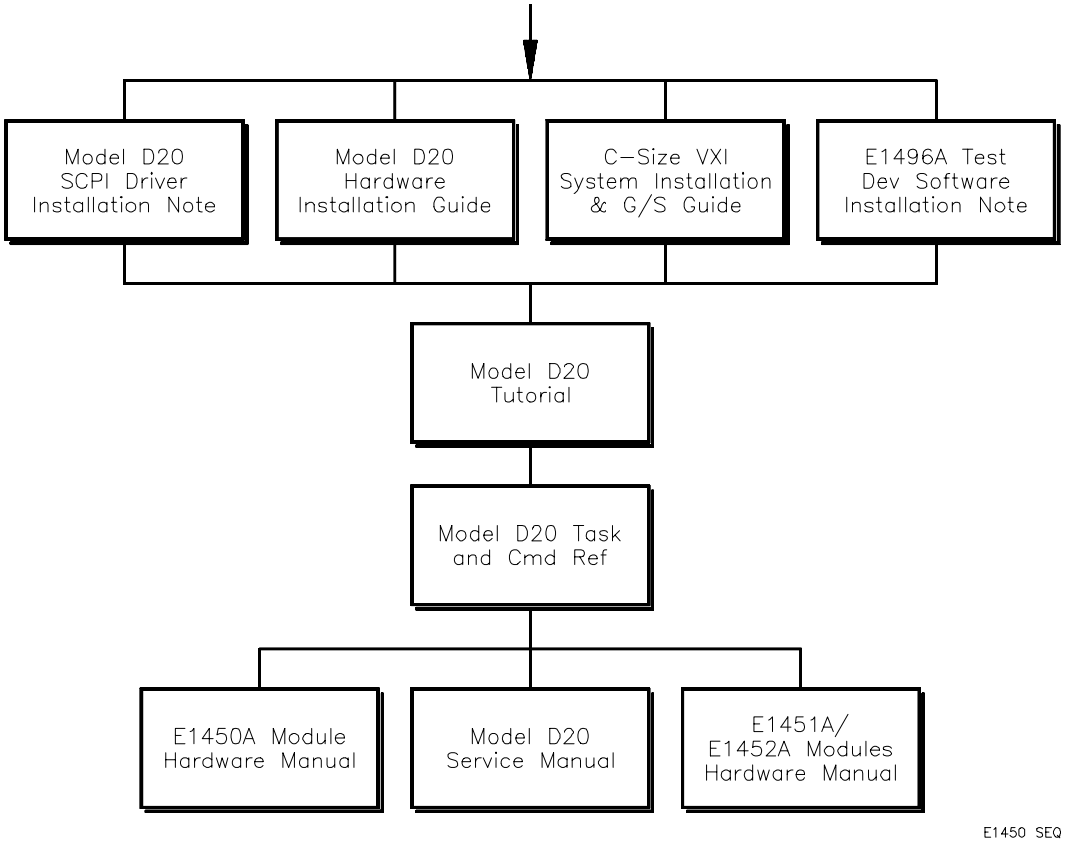
Product Regulations Program Manager

For further information, please contact your local Agilent Technologies sales office, agent or distributor.
Authorized EU-representative: Agilent Technologies Deutschland GmbH, Herrenberger Strabe 130, D 71034 Böblingen, Germany

Model D20 Documentation

Suggested Sequence to Use Manuals/Notes



Manuals/Notes Descriptions

Manual/Note Title	Description
SCPI Driver Installation Note	Shows how to Install downloadable SCPI drivers in Agilent E1405B
Model D20 Hardware Installation Guide	Shows how to Install and configure the Model D20
E1496A Software Installation Note	Shows how to Install Agilent E1496A Test Development Software
VXI System Installation and Getting Started Guide	Shows how to configure Agilent E1400B M/F & E1405B Cmd Module
Model D20 Tutorial	Shows how to get started using the Model D20
Model D20 Task/Command Reference	Shows typical tasks and commands for the Model D20
Model D20 Service Manual	Shows how to service the Model D20
E1450A Hardware Manual	Describes Agilent E1450A Timing Module hardware
E1451A/52A Hardware Manual	Describes Agilent E1451A/52A Pattern Modules hardware
Model D20 CLIP	Model D20 schematics, component locators, and parts lists

What's in this Manual

Manual Overview

This manual shows how to service the Agilent 75000 Series C Model D20 Digital Functional Test System (Model D20). See *Model D20 Documentation*, page *v*, for additional manuals that may be required to service the Model D20.

Manual Content

Chap	Title	Content
1	General Information	Lists basic Model D20 description, tools and test equipment required for service, and procedures to inspect and ship the Model D20.
2	Verification Tests	Describes self-test, functional verification, and performance verification tests for the Model D20.
3	Replaceable Parts	Lists part numbers for user-replaceable parts in the Model D20. Provides information on ordering spare parts and module exchange.
4	Service	Procedures to aid in fault isolation and repair of the Model D20.
5	DIAGnostic Commands	Describes the DIAGnostic commands for use in servicing the Model D20.

Contents

Chapter 3 - Replaceable Parts

Chapter 4 - Service

Chapter 5 - DIAGnostic Commands

Index

1
General Information

Introduction

This service manual contains information to test, troubleshoot, and repair the Agilent 75000 Series C Model D20 Digital Functional Test System (Model D20). Figure 1-1 shows a typical Model D20.

NOTE

See "Model D20 Documentation", page iv, for a list of manuals that describe Model D20 operation and hardware. The information in this manual assumes you are familiar with Model D20 operation. If incoming inspection is required, see "Inspection/Shipping" in this chapter.

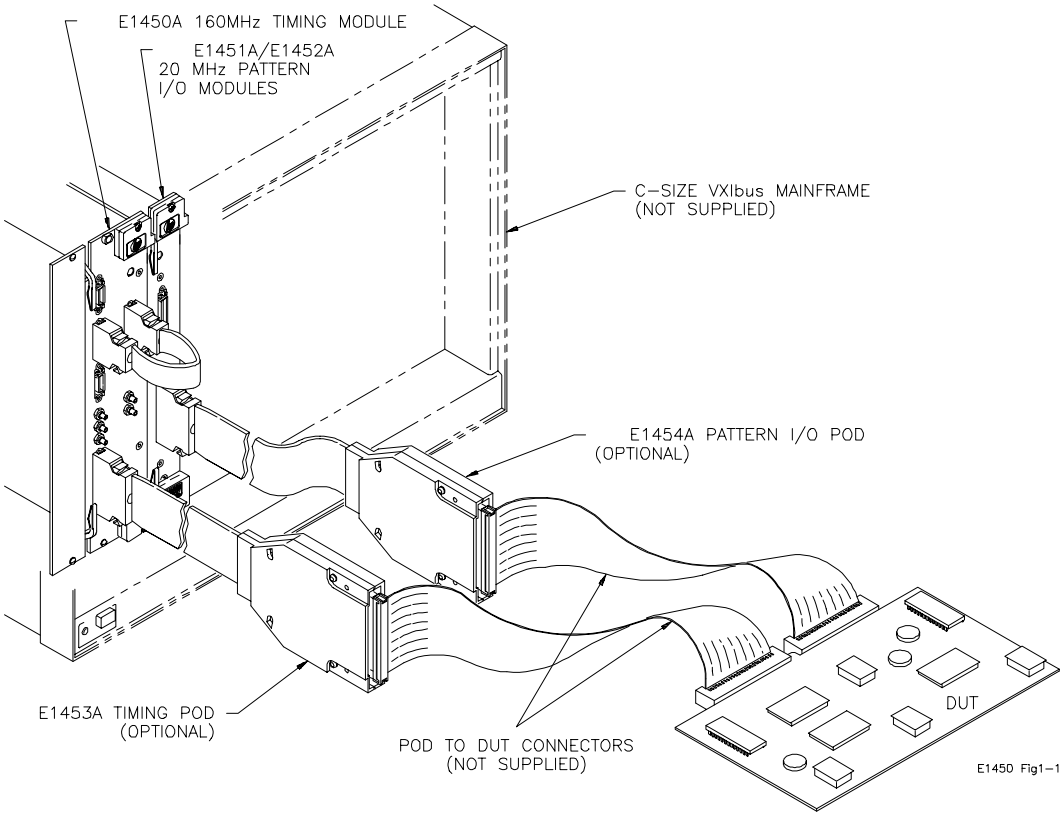


Figure 1-1. Typical Model D20 Configuration

Safety Information

The Model D20 is a Safety Class I instrument that is provided with a protective earth terminal when installed in the mainframe. Check the mainframe, Model D20, and all related documentation for safety markings and instructions before operating or servicing the Model D20.

See the WARNINGS page (page iii) for a summary of safety information. Safety information to test and service the Model D20 follows and is also found throughout this manual.

Model D20 WARNINGS

Follow the WARNINGS listed to avoid possible injury to yourself or others when operating, repairing, or servicing the Model D20.

WARNING

SERVICE-TRAINED PERSONNEL ONLY. The information in this manual is for service-trained personnel who are familiar with electronic circuitry and are aware of the hazards involved. To avoid personal injury or damage to the instrument, do not perform procedures in this manual or do any servicing unless you are qualified to do so.

CHECK MAINFRAME POWER SETTINGS. Before applying power, verify that the mainframe setting matches the line voltage and the correct fuse is installed. An uninterruptible safety earth ground must be provided from the main power source to the supplied power cord set.

GROUNDING REQUIREMENTS. Interruption of the protective (grounding) conductor (inside or outside the mainframe) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury. (Grounding one conductor of a two-conductor outlet is not sufficient protection.)

IMPAIRED PROTECTION. Whenever it is likely that instrument protection has been impaired, the mainframe must be made inoperative and be secured against any unintended operation.

REMOVE POWER IF POSSIBLE. Some procedures in this manual may be performed with power supplied to the mainframe while protective covers are removed. Energy available at many points may, if contacted, result in personal injury. (If service can be performed without power applied, remove the power.)

WARNING

USING AUTOTRANSFORMERS. If the mainframe is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to neutral (that is, the grounded side of the main's supply).

USE PROPER FUSES. For continued protection against fire hazard, replace the line fuse(s) only with fuses of the same current rating and type (such as normal blow, time delay, etc.). Do not use repaired fuses or short-circuited fuseholders.

Model D20 CAUTIONS

Follow the CAUTIONS listed to avoid possible damage to the equipment when performing instrument operation, service, or repair.

CAUTION

MAXIMUM VOLTAGE. Maximum positive voltage that may be applied to the Ready In or TTL Trig In terminals of an Agilent E1450A Timing Module is +5V. Maximum negative voltage that may be applied to the ECL Trig In terminals of an Agilent E1450A Timing Module is -5V.

STATIC ELECTRICITY. Static electricity is a major cause of component failure. To prevent damage to the electrical components in the Model D20, observe anti-static techniques when removing a Model D20 module from the mainframe or when working on a Model D20 module. Also, be sure to tighten the front panel screws when installing a Model D20 module in a mainframe slot.

Product Information

This section lists Model D20:

- specifications
- serial number information
- options
- service kit information
- service programs disk information
- component level information package (CLIP)
- environmental limits
- recommended test equipment

Specifications

See *Appendix A - Specifications* in the *Model D20 Task and Command Reference Manual* for Model D20 specifications.

Serial Numbers

Figure 1-2 shows Agilent Technologies serial number structure. Model D20 modules covered by this manual are identified by the serial number prefixes listed on the title page.

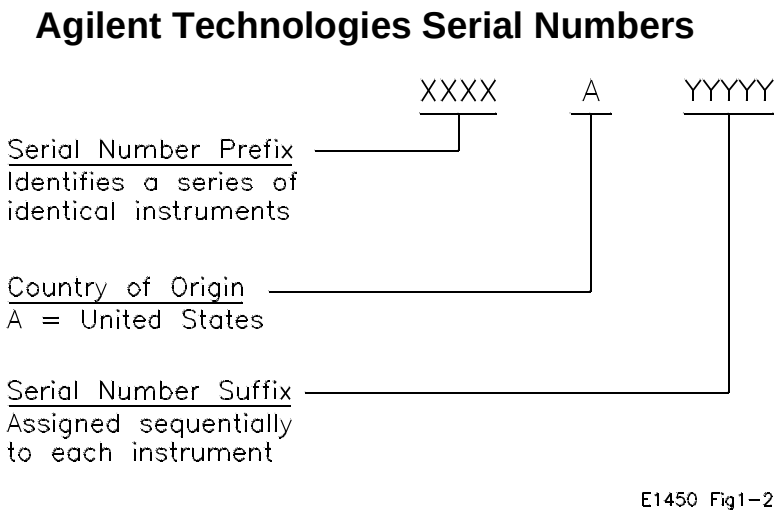


Figure 1-2. Agilent Technologies Serial Numbers

Options

Model D20 components can be ordered separately or as part of a Digital Functional Test System (Agilent E1493A) or Digital Test Development System (Agilent E1494A). See the *Agilent Technologies 75000 Family of VXI Products* catalog for option information.

Service Programs Disk

Included with this service manual is a *Model D20 Service Programs* disk. This disk contains example programs for the self-tests and verification tests described in *Chapter 2 - Verification Tests*, for the service routines in *Chapter 4 - Service*, and for the DIAGnostic command examples in *Chapter 5 - DIAGnostic Commands*. The programs on the disk are in LIF format, and the disk is intended for use in HP 9000 Series 200/300 (or equivalent) computers. The disk has four files:

- **FUNC_VER** for self-test and functional verification tests
- **PERF_VER** for performance verification tests
- **SERV_TST** for service (troubleshooting) tests
- **DIAG_CMD** for DIAGnostic command examples

To run a self-test, functional verification test, performance verification test, service test, or DIAGnostic command example:

- insert the *Model D20 Service Programs* disk in your disk drive
- load the file with LOAD "file_name"
- press RUN
- select the test/example desired

Component Level Information Packet (CLIP)

A Component Level Information Packet (CLIP) for the Model D20 is available from Agilent Technologies (part number E1493-90033). Contact your local Agilent Technologies Sales and Support Office for ordering information.

Operating/Storage Environments

The Model D20 should be stored in a clean, dry environment. See Table 1-1 for recommended Model D20 operating/storage environments.

Table 1-1. Model D20 Environments

	Temperature	Relative Humidity
Operating Environment	0°C to +55°C	<65% (0 °C to +40°C)
Storage/ Shipment	-40°C to +75°C	<65% (0°C to +40°C)

Recommended Test Equipment

See Table 1-2 for test equipment recommended to test and service the Model D20. Essential requirements for each piece of test equipment are listed in the *Requirements* column. You may substitute other equipment if it meets the requirements in Table 1-2.

Table 1-2. Model D20 Recommended Test Equipment

Instrument	Requirements	Recommended Model	Use*
Controller, GPIB	GPIB compatibility as defined by IEEE Standard 488-1987 and the identical ANSI Standard MC1.1: SH1, AH1, T2, TE0, L2, LE0, SR0, RL0, PP0, DC0, DT0, and C1, 2, 3, 4, 5	HP 9000 Series 300	F,O, P,T
Mainframe	Compatible with Model D20	E1400B/E1400T (requires Agilent E1405 Command Module)	F,O, P,T
Digital Multimeter	Voltage Range: ±10 VDC Current Range: ±20 mA DC Accuracy: ±(.015% reading + 1 mV) ±(.02% reading + 1 μA)	Agilent 3458A, Agilent 3478A or Agilent E1411B	F,O, P,T
Digitizing Oscilloscope	Bandwidth: 60 MHz Vertical Sensitivity: 1V/div Vertical input: 5V External Trigger Capability	Agilent 54111D or Agilent 54123T	F,T
Universal Counter	Frequency Range: 12 MHz Accuracy: ±0.001%	Agilent 5334B	P

*F = Functional Verification Tests, O = Operation Verification Tests, P = Performance Verification Tests, T = Troubleshooting

Inspection/ Shipping

This section shows initial (incoming) inspection and shipping guidelines for the Model D20.

Initial Inspection

Use the steps in Figure 1-3 as guidelines to perform initial (incoming) inspection of the Model D20.

WARNING

To avoid possible hazardous electrical shock, do not perform electrical tests if there are signs of shipping damage to the shipping container or to the instrument.

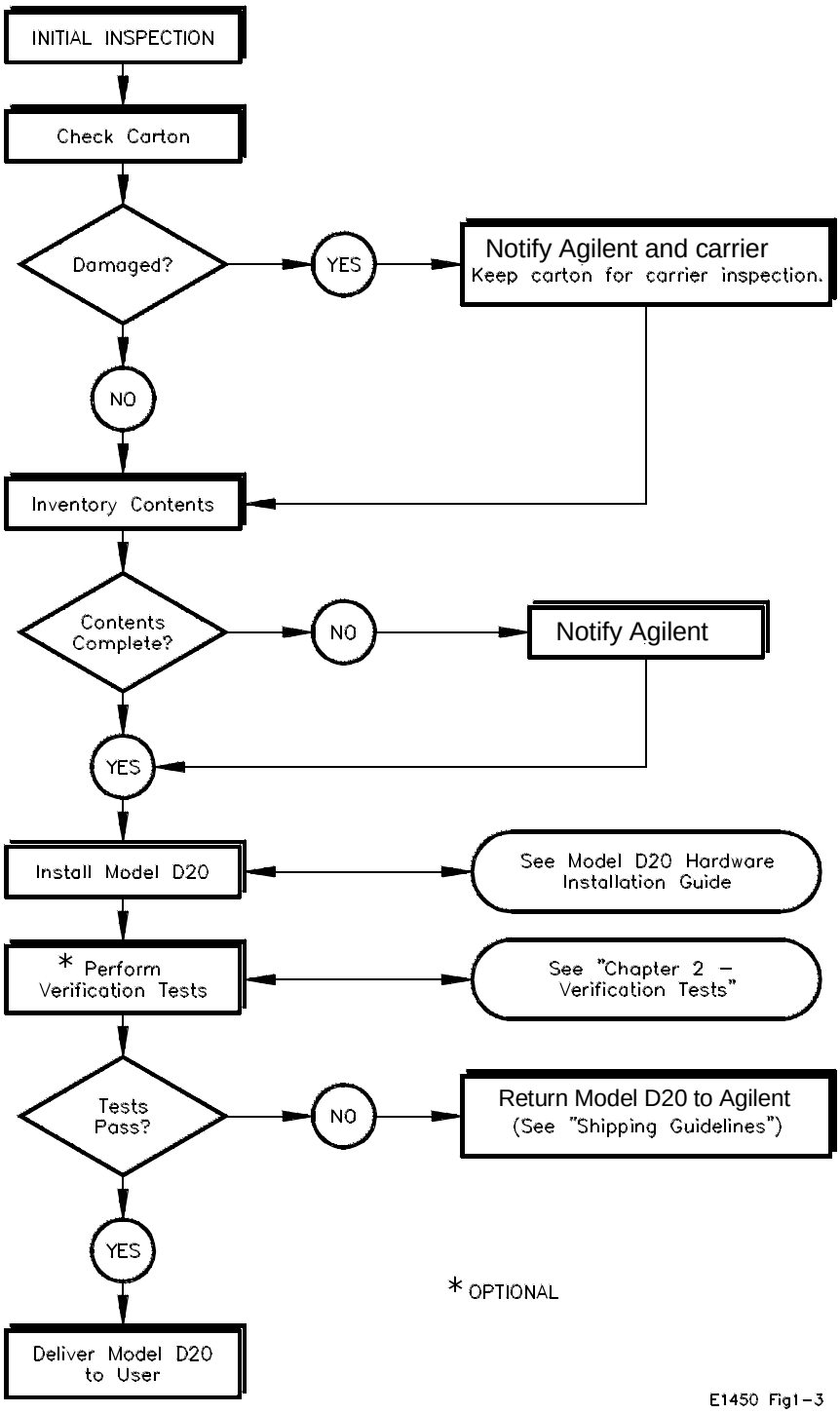
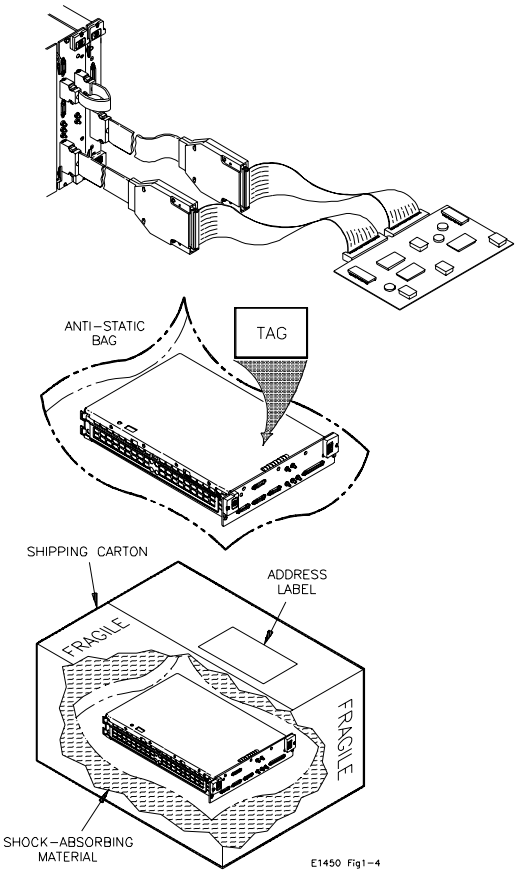


Figure 1-3. Initial (Incoming) Inspection Guidelines

Shipping Guidelines

Follow the steps in Figure 1-4 to return Model D20 modules/pods to an Agilent Technologies Sales and Service Office or Service Center.

SHIPPING GUIDELINES



1 Remove Cables/Connectors/DUTs

- Remove DUTs from modules/pods
- Remove pods from modules
- Remove cables/connectors from modules/pods

2 Prepare Module/Pod

- Attach tag to module/pod that identifies
  - owner
  - Model Number/Serial Number
  - Service Required
- Place tagged device in anti-static bag

3 Package Module/Pod

- Place packaged module in shipping carton*
- Place 75 to 100 mm (3 to 4 inches) of shock-absorbing material around the module/pod
- Seal the shipping carton securely
- Mark the shipping carton FRAGILE

4 Ship Module/Pod to Agilent Technologies

- Place address label on shipping carton **
- Send carton to Agilent Technologies

*We recommend you use the same shipping materials as those used in factory packaging (available from Agilent Technologies). For other (commercially-available) shipping materials, use a double-wall carton with minimum 2.4 MPa (350 psi) test.

Figure 1-4. Recommended Shipping Guidelines

2
Verification Tests

Introduction

This chapter describes Model D20 self-tests, functional verification tests, and performance verification tests. (There are no user adjustments for the Model D20.) Table 2-1 defines Model D20 verification tests and suggests when to use each type.

WARNING

Do not perform any of the verification tests in this chapter unless you are a qualified, service-trained person and have read the WARNINGS and CAUTIONS in Chapter 1.

NOTE

Specifications listed in Appendix A - Specifications of the Model D20 Task and Command Reference, but not tested in this chapter, are defined to be "Guaranteed by Design" (not required to be tested) if the Model D20 passes the performance verification tests in this chapter.

Table 2-1. Model D20 Verification Test Definitions

Title	Description	When to Use:
Self-Tests	Use power-on or TEST? to verify that the Model D20 is operational and is communicating with the computer.	When you want to verify operation and/or communication.
Functional Verification Tests	Gives a high probability that the Model D20 is functional. These tests provide a PASS/FAIL result.	At incoming inspection, after module repair, or whenever faulty operation is suspected.
Performance Verification Tests	Verifies that the Model D20 meets all testable specifications. These tests PASS if the result is within defined limits, or FAIL if the result is outside the defined limits.	At incoming inspection or at yearly intervals (more often in harsh environments).

Test Conditions/ Procedures

The test administrator must know Model D20 and test equipment operation. It is assumed that a qualified, service-trained person will connect cables and adaptors required. See Table 1-2, *Recommended Test Equipment*, for test equipment requirements. Performance verification tests should be done at least once a year. For severe operating environments, do the performance tests more often.

Performance Test Record

Table 2-3, *Model D20 Performance Test Record*, at the end of this chapter, provides space to enter the results of each verification test. You can make a copy of this table if desired.

Using the Light Board

Most verification tests in this chapter use a Light Board to show verification program results. See Figure 2-1 for typical Light Board connections. As required, each verification test shows specific connections to the Light Board.

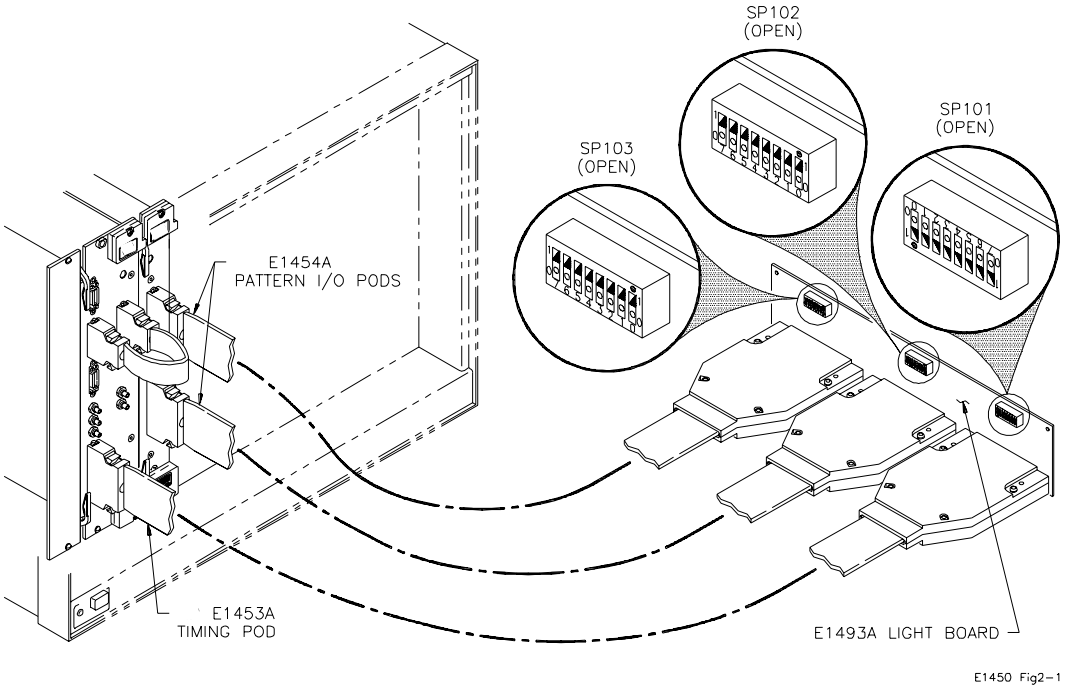


Figure 2-1. Typical Light Board Connections

Model D20 Self-Tests

This section shows how to perform Model D20 self-tests using the power-on (SYST:ERR?) and/or hardware (TEST?) commands. Either test is usually adequate to verify that the Model D20 is operational. If a self-test fails, see *Chapter 4 - Service* for further tests/information.

NOTE

The TEST? command is not guaranteed to find all hardware faults. It does, however, provide more testing of the Model D20 hardware than the power-on test.

Test S-1: Model D20 Power-On Test

Description

This test uses the SYST:ERR? command for the Model D20 power-on test. A "+0, no error" return indicates the test passed.

Set up Equipment

- Turn mainframe power OFF
- Connect computer to mainframe (see Figure 2-2)
- Turn mainframe power ON

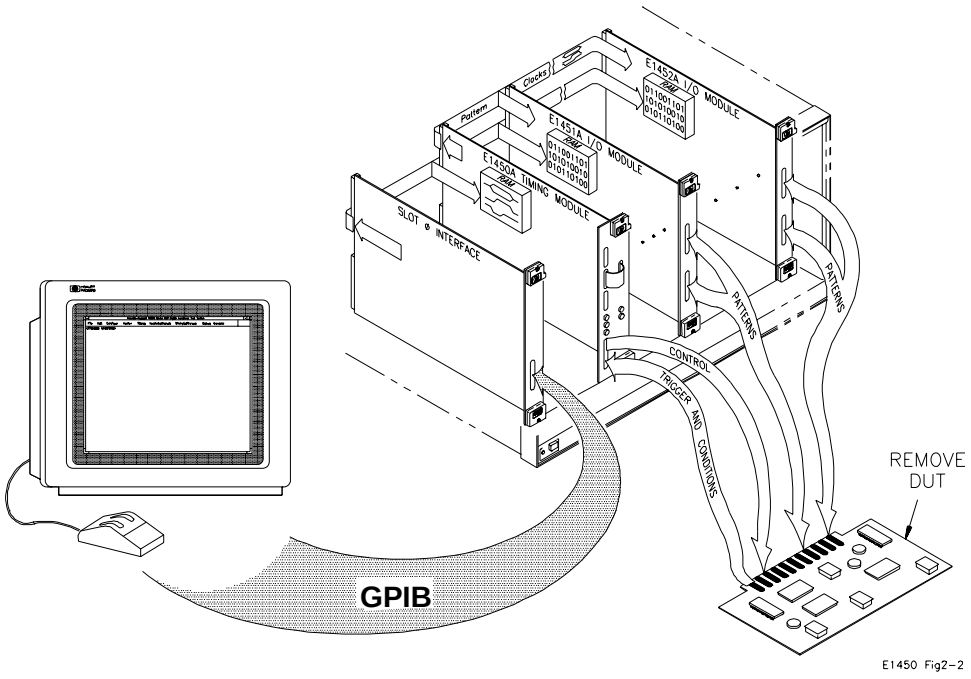


Figure 2-2. Model D20 Self-Test Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test S-1: Model D20 Power-on Test"

Example Program

This program performs a power-on test for the Model D20 using the SYST:ERR? command. If the power-on test passes, +0,"No error" is returned. If the power-on test fails, the test returns an error message for each error detected.

```
1     !Test S-1: Power-On Test
2     ! ---------------------------------------- Initial Assignments ----------------------------------------------------
10    CLEAR SCREEN
20    ON TIMEOUT 7,5 GOSUB Comm_err                    !GPIB timeout error after 5 seconds
30    ASSIGN @Dft TO 70917                             !Model D20 address is 70917
40    DIM A$[100]
50    DISP CHR$(129)                                   !Inverse video on display
60    PRINT "Test S-1: Power-On Test"
70    PRINT
80    DISP " Turn Mainframe Power OFF then ON. Then, press Continue. "
90    PAUSE
100   CLEAR SCREEN
110   CLEAR @Dft
120   OUTPUT @Dft;"*RST"                               !Send reset to Model D20
121   !------------------------------ Power-on error checks ------------------------------------------------------
130   WHILE A$<>"+0,""No error"""                      !Begin power-on error checks
140     OUTPUT @Dft;"SYST:ERR?"                        !Check for system errors
150     ENTER @Dft;A$                                  !Enter errors
160     PRINT "Power-on Errors = ";A$                  !Display errors
170   END WHILE
180   OUTPUT @Dft;"*CLS"                               !Clear status register
190   IF A$="+0,""No error""" THEN
200     GOSUB Test_ok                                  !Go to test PASSED indication
210   ELSE
220     GOSUB Pwr_on_errs                              !Go to error indication
230   END IF
231   ! ------------------------------ GPIB Communication Failure Message -----------------------------------
240 Comm_err:   !
250   CLEAR SCREEN
260   BEEP
```

(continued on next page)

```
270   PRINT "GPIB communication check failed."                    !GPIB communication failure
280   PRINT
290   PRINT "The Model D20 is not responding. Check GPIB address"
300   PRINT "of Model D20 modules, the GPIB interface cable, and"
310   PRINT "the Agilent E1405B Command Module."
320   PRINT
330   DISP " Restart program when error(s) are corrected. "
340   OFF TIMEOUT 7                                               !Clear GPIB timeout
350   STOP
351   ! ------------------------------ Power-on error messages ----------------------------------------
360 Pwr_on_errs:   !
370   BEEP
380   DISP " Correct power-on errors listed.  Then, rerun this program. "
390   STOP
391   ! --------------------------------- Successful test completion ---------------------------------
400 Test_ok:   !
410   PRINT "Model D20 Power-on test passed"
420   DISP CHR$(128)                                              !Normal video on display
430   OFF TIMEOUT 7                                               !Clear GPIB timeout
440   END
```

Typical Result A typical result for no power-on errors is:

```
Power-on Errors = +0,"No error"
Model D20 Power-on test passed
```

Test S-2: Model D20 Hardware Test

Description

This test uses the TEST:MODule? command to make a hardware check of all installed Model D20 modules. See the TEST command in *Chapter 4 - Command Reference* of the *Model D20 Task and Command Reference* for command information and error messages.

CAUTION

Disconnect all DUTs before executing the TEST? command. The Model D20 will change RESPonse ports to STIMulus ports during the test which may damage any connected DUTs.

Set up Equipment

- Turn mainframe power OFF
- Connect computer to mainframe (see Figure 2-3)
- Disconnect ALL DUTs from Model D20
- Turn mainframe power ON

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"

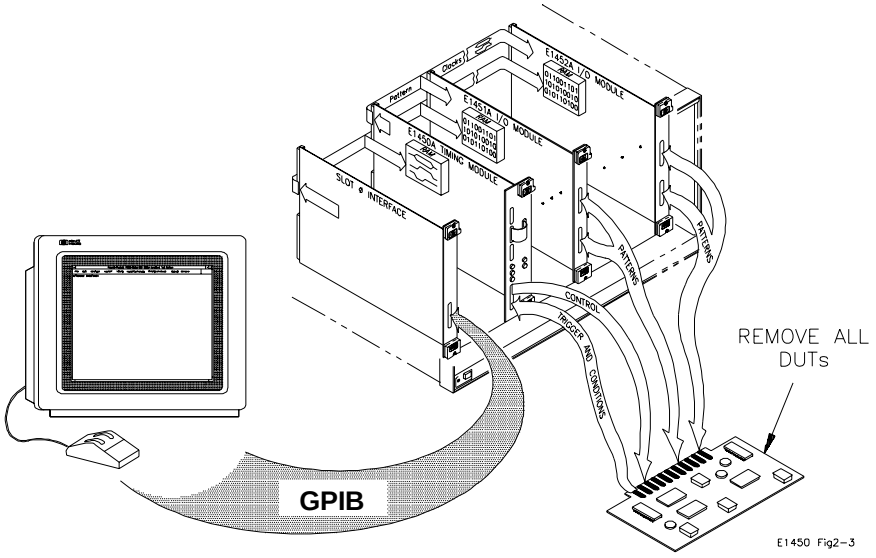


Figure 2-3. Model D20 Hardware Test Connections

- Press RUN
- Select "Test S-2: Model D20 Hardware Test"

Example Program

This program tests all installed Model D20 modules using the TEST:MODule? command to find all modules with detected faults.

```
1     !Test S-2: Model D20 Hardware Test
2     !
10    ASSIGN @Dft to 70917                                    !Default address = 70917
20    PRINT "Test S-2: Model D20 Hardware Test"
30    PRINT
40    INPUT " Enter number of modules installed (including Timing Module) ",Number!Enter no. of modules
50    ALLOCATE Fault_code$(Number)[100]                       !Allocate memory
60    FOR I=0 TO Number-1                                     !Begin loop
70       OUTPUT @Dft;"TEST:MOD? ";I                           !Output TEST:MODule? command
80       ENTER @Dft;Fault_code$(I)                            !Enter results
90       IF Fault_code$(I)="+0,+0,+0,+0" THEN                 !No faults on module
100         PRINT "Test PASSED for module ";I                 !Test PASSED indication
110      ELSE
120         PRINT "Fault code for module ";I;"= ";Fault_code$(I)  !Display fault code
130      END IF
140   NEXT I                                                  !Next module
150   END
```

Typical Results

If a module passes the hardware test, the display is Test PASSED for module *i*. Assuming two modules are installed, if module 0 passes the test, but module 1 fails the test (port 2 address counter failed), the display is:

```
Test PASSED for module 0
 Fault code for module 1 = +0,+0,+10,+0
```

Functional Verification Tests

This section describes functional verification tests for the Model D20. These (optional) tests can be used to check specific Model D20 functions. The tests are valid ONLY if an Agilent E1450A Timing Module is used.

Typically, functional verification tests are used after repair or whenever Model D20 operation is questionable. Table 2-2 lists functional verification tests for the Model D20.

Table 2-2. Model D20 Functional Verification Tests

Test #	Test Title	Checks This Model D20 Function
F-1 F-2 F-3	Generating Patterns Recording Patterns Comparing Patterns	Pattern Generation Pattern Recording Pattern Comparison
F-4 F-5 F-6	Control Outputs Trigger Test Condition Inputs	Control Outputs Trigger Inputs Condition (Q) Inputs
F-7 F-8 F-9	Marker Outputs End-if-Ready Inputs Clock Outputs	Marker Outputs End-If-Ready Inputs STIMulus/RESPonse Clocks

Test F-1: Generating Patterns

Description

This test generates patterns on a selected port of a Pattern I/O Module. The pattern output sequentially lights LEDs (from 0 to 7) for the selected port on the Light Board. You can use this test to check the STIMulus output of the Model D20.

Set up Equipment

- Turn mainframe power OFF
- Make Light Board connections (see Figure 2-4)
- Turn mainframe power ON

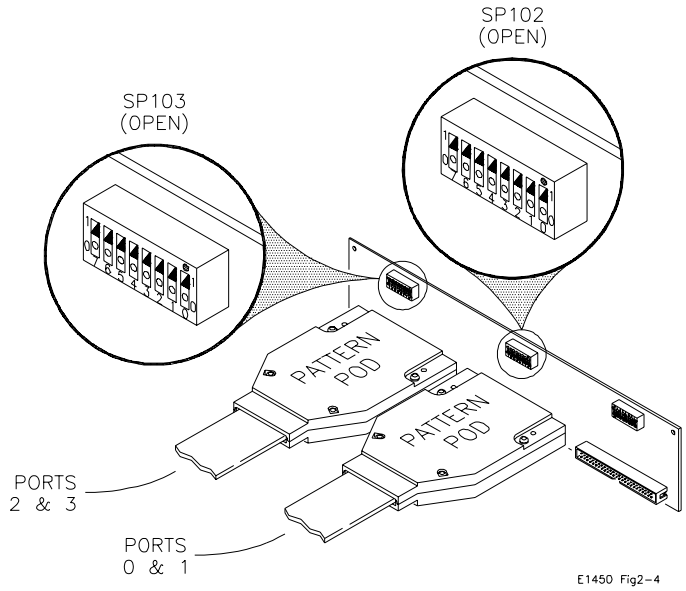


Figure 2-4. Test F-1: Generating Patterns Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-1: Generating Patterns"

Example Program This program outputs a STIMulus pattern on a selected port of a Pattern I/O Module. The pattern sequentially lights each Light Board LED (from 0 to 7) for the selected port.

```
1    ! Test F-1: Generating Patterns
2    !
3    ! ---------- Initial Assignments ----------
10     ASSIGN @Dft TO 70917                          !Model D20 address = 70917
20     DISP CHR$(129)                                !Inverse video on display
30     PRINT "Test F-1: Generating Patterns"
40     PRINT
41   ! ---------- Select Module Number ----------
50     INPUT " How many Pattern I/O modules are installed?  ",Mods   !Enter number of
                                                                       pattern I/O modules
60   Retry_mod:     !
70     INPUT " Enter module number (1,2,...) of Pattern I/O          !Enter pattern I/O module number
             module to be tested ",Mod_no
80     IF Mod_no<1 OR Mod_no>Mods THEN
90         BEEP
100        PRINT TABXY(1,15),"Invalid module number.                 !Invalid module number entry warning
                              Please reenter module number."
110        GOTO Retry_mod
120    END IF
130    CLEAR SCREEN
131  ! ---------- Select Port Number ----------
140  Retry_port:    !
150    INPUT " Enter port number (0,1,2, or 3) to be tested ",Port_no   !Enter number of port to be tested
160    IF Port_no<0 OR Port_no>3 THEN
170       BEEP
180       PRINT TABXY(1,15),"Invalid port number.                  !Invalid port number entry warning
                             Please reenter port number."
190       GOTO Retry_port
200    END IF
210    CLEAR SCREEN
211  !---------- Set  up Sequence ----------
220    Number$=","&"("&"@"&VAL$(Mod_no)&"("&VAL$(Port_no)&"))"  !Address indicator for module
                                                                  and port selected
230    OUTPUT @Dft;"*RST"                            !Set instrument to known condition
240    OUTPUT @Dft;"SEQ:DEL:ALL"                     !Delete all previous sequences
250    OUTPUT @Dft;"SEQ:DEF TEST_1,9"                !Define seq "TEST_1" with 9 vectors
260    OUTPUT @Dft;"SEQ TEST_1"                      !Select "TEST_1" sequence
```

(continued on next page)

```
261  ! ---------------------------------------- Define Pin Group ----------------------------------------------------
270  OUTPUT @Dft;"GRO:DEL:ALL"                                   !Delete all previous pin groups
280  OUTPUT @Dft;"GRO:DEF DATA_OUT";Number$                      !"DATA_OUT" pin group
290  OUTPUT @Dft;"GRO DATA_OUT"                                  !Select group "DATA_OUT"
300  OUTPUT @Dft;"GRO:MODE STIM"                                 !Set group to STIMulus mode
310  OUTPUT @Dft;"STIM:PATT:SEQ:PART 0,1,2,4,8,16,32,64,128,0"!Load STIMulus data pattern
320  OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                           !Use internal STIMulus clock 0
321  !---------------------- Set up Timing Cycle and Resolution ------------------------------------------
330  OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                              !Delete all previous timing cycles
340  OUTPUT @Dft;"TIM:CYCL:DEF TC_1,750"                         !Timing cycle "TC_1" has 750 subcycles
350  OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,9,TC_1"                     !Assign "TC_1" to each vector
360  OUTPUT @Dft;"TIM:RES 400E-6"                                !Each subcycle = 400 usec
361  ! ---------------------------------------- RUN Program ---------------------------------------------------
370  PRINT "Test F-1: Generating Patterns"
380  PRINT
390  PRINT  "1.  Make sure switches SP102 and SP103 are OPEN."
400  PRINT
410  PRINT  "2.  When this test is RUN, port";Port_no;"LEDs should light"
420  PRINT  "     sequentially from 0 through 7 and then turn OFF"
430  DISP  " Press Continue when ready to observe the LEDs "
440  PAUSE
450  CLEAR SCREEN
460  OUTPUT @Dft;"RUN"                                           !RUN program
470  END
```

Typical Results For this program, the LEDs on the selected port should light sequentially from 0 through 7.

Test F-2: Recording Patterns

Description

This test outputs STIMulus patterns via a selected port of a Pattern I/O Module and records the patterns via a second port of the module. The recorded patterns are then read and printed. If the recorded patterns are identical to the STIMulus patterns, the test passes. You can use this test to check the record capabilities of the Model D20.

Set up Equipment

- Turn mainframe power OFF
- Make Light Board connections (see Figure 2-5)
- Turn mainframe power ON

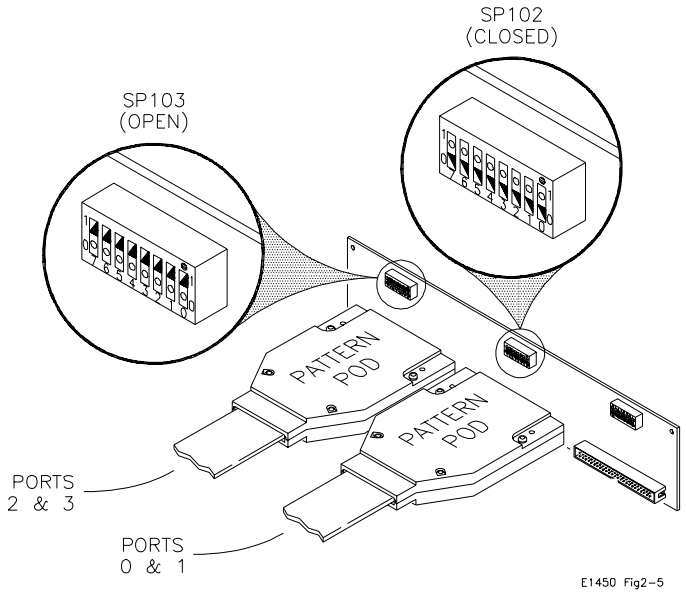


Figure 2-5. Test F-2: Recording Patterns Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-2: Recording Patterns"

Example Program This program outputs a STIMulus pattern sequence (1, 2, 4, 8, 16, 32, 64, 128, 0) on a selected port of a Pattern I/O Module and records that sequence via a second selected port. The recorded pattern sequence is then queried.

```
1     ! Test F-2: Recording Patterns
2     !
3    !---------------------------------------------- Initial Assignments ----------------------------------------------------
10    ASSIGN @Dft TO 70917                                          !Model D20 Address = 70917
20    DISP CHR$(129)                                                !Inverse video on display
30    CLEAR SCREEN
40    PRINT "Test F-2: Recording Patterns"
50    PRINT
60    INPUT " How many Pattern I/O modules are installed? ",Mod     !Nbr of Pattern I/O modules
70  Retry_mod:     !
80    INPUT " Select module number (1,2,...) of Pattern I/O         !Select module to be tested
              module to be tested ",Mod_no
90    IF Mod_no<1 OR Mod_no>Mod THEN
100     PRINT TABXY(1,16)," Invalid module number. Please reenter   !Invalid module number warning
                          module number. "
110     BEEP
120     GOTO Retry_mod
130   END IF
140   CLEAR SCREEN
150 Retry_stim_port:    !
160    INPUT " Select STIMulus port number (0, 1, 2, or 3) ",Stim_port   !Select STIMulus port number
170    IF Stim_port<0 OR Stim_port>3 THEN
180      PRINT TABXY(1,16),"Invalid STIMulus port number. Please    !Invalid STIMulus port nbr warning
                          reenter port number"
190      BEEP
200      GOTO Retry_stim_port
210    END IF
220    IF Stim_port=0 THEN Resp_port=1                               !STIM port 0, RESP port 1
230    IF Stim_port=1 THEN Resp_port=0                               !STIM port 1, RESP port 0
240    IF Stim_port=2 THEN Resp_port=3                               !STIM port 2, RESP port 3
250    IF Stim_port=3 THEN Resp_port=2                               !STIM port 3, RESP port 2
260    CLEAR SCREEN
261    !---------------------------------------------- Set up Sequence ---------------------------------------------------
270    Data_out$=","&"("&"@"&VAL$(Mod_no)&"("&VAL$(Stim_port)&"))"   !STIMulus port address
280    Data_in$=","&"("&"@"&VAL$(Mod_no)&"("&VAL$(Resp_port)&"))"    !RESPonse port address
290   OUTPUT @Dft;"*RST"                                            !Set instrument to known condition
300   OUTPUT @Dft;"SEQ:DEL:ALL"                                     !Delete all previous sequences
310   OUTPUT @Dft;"SEQ:DEF TEST_1,9"                                !Define seq "TEST_1" with 9 vectors
```

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```
320  OUTPUT @Dft;"SEQ TEST_1"                                    !Select "TEST_1" sequence
321  ! ---------------------------- Set up STIMulus Group ----------------------------------------------------
330  OUTPUT @Dft;"GRO:DEL:ALL"                                   !Delete all previous pin groups
340  OUTPUT @Dft;"GRO:DEF DATA_OUT";Data_out$                    !Define "DATA_OUT" group
350  OUTPUT @Dft;"GRO DATA_OUT"                                  !Select group "DATA_OUT"
360  OUTPUT @Dft;"GRO:MODE STIM"                                 !Set group to STIMulus mode
370  OUTPUT @Dft;"STIM:PATT:SEQ:PART 0,1,2,4,8,16,32,64,128,0"   !Load STIMulus pattern
380  OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                           !Use internal STIMulus clock 0
381  ! ----------------------------------- Set up RESPonse Group ------------------------------------------
390  OUTPUT @Dft;"GRO:DEF DATA_IN";Data_in$                      !Define "DATA_IN" pin group
400  OUTPUT @Dft;"GRO DATA_IN"                                   !Select "DATA_IN" pin group
410  OUTPUT @Dft;"GRO:MODE RESP"                                 !Set group to RESPonse mode
420  OUTPUT @Dft;"RESP:CLOC:SOUR INT0"                           !Use internal RESPonse clock 0
430  OUTPUT @Dft;"RESP:COMP OFF"                                 !Enable record mode (by disabling
                                                                 compare mode)
431  !-------------------------- Set up Timing Cycle and Resolution ----------------------------------------
440  OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                              !Delete previous timing cycles
450  OUTPUT @Dft;"TIM:CYCL:DEF TC_1,750"                         ! "TC_1" has 750 subcycles
460  OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,9,TC_1"                     !Assign "TC_1" to each vector
470  OUTPUT @Dft;"TIM:RES 400E-6"                                !Each subcycle = 400 usec
480  OUTPUT @Dft;"TIM:CYCL TC_1"                                 !Select timing cycle "TC_1"
490  OUTPUT @Dft;"TIM:CYCL:RPCL0 1"                              !Delay RESP clock 1 subcycle
500  CLEAR SCREEN
501 !-----------------------------------------------RUN the Program ----------------------------------------
510   PRINT  "1.  Make sure switches SP102 and SP103 are OPEN."
520   PRINT
530   PRINT  "2. When this program is RUN, the LEDs on STIMulus port";Stim_port;"and"
540   PRINT  "    RESPonse port";Resp_port;"should light sequentially from 0 through"
550   PRINT  "    7 and then turn OFF."
560   DISP " Press Continue when ready to observe the LEDs "
570   PAUSE
580  OUTPUT @Dft;"RUN"                                           !RUN program
590  CLEAR SCREEN
600  WAIT 3
610  OUTPUT @Dft;"STOP"                                          !STOP Model D20
611  ! ------------------------ Check DATA_IN response pattern ---------------------------------------
620  DIM A$[256]
630  OUTPUT @Dft;"GRO DATA_IN"                                   !Select RESPonse pin group
640  OUTPUT @Dft;"RESP:PATT:SEQ:PART? 0,9"                       !Check RESPonse pin group pattern
650  ENTER @Dft;A$                                               !Enter pattern
```

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```
660  CLEAR SCREEN                                                    !Display pattern
661  !---------------------------------------- Display Results ----------------------------------------
670  PRINT "Test F-2: Recording Patterns Results"
680  PRINT
680  PRINT "STIMulus pattern on port";Stim_port;"= +1,+2,+4,+8,+16,+32,+64,+128,+0"
690  PRINT "RESPonse pattern on port";Resp_port;" =  ";A$
700  PRINT  "                          NOTE"
710  PRINT
720  PRINT  "If the RESPonse pattern does not match the STIMulus pattern,"
730  PRINT  "make sure SP102 (ports 0 and 1) or SP103 (ports (2 and 3) is"
740  PRINT  "OPEN. If not, OPEN the switch and rerun this test."
750  END
```

Typical Result

As the test RUNs, the selected port's LEDs should light sequentially (from 0 to 7). When the test completes, the selected port's LEDs should be OFF. A typical result for RESPonse port 1 is:

```
Test F-2: Recording Patterns

STIMulus pattern on port  1   = +1,+2,+4,+8,+16, +32,+64,+128,+0
RESPonse pattern on port 1  = +1,+2,+4,+8,+16,+32,+64,+128,+0
```

Test F-3: Comparing Patterns

Description

This test outputs a STIMulus pattern (55) via a selected STIMulus port of a Pattern I/O Module and an identical RESPonse pattern (55) via a selected RESPonse port of the module. The RESPonse pattern and STIMulus pattern are then compared. If the patterns are identical, the test passes. You can use this test to check the Model D20 compare function.

Set up Equipment

- Turn mainframe power OFF
- Make Light Board connections (see Figure 2-6)
- Turn mainframe power ON

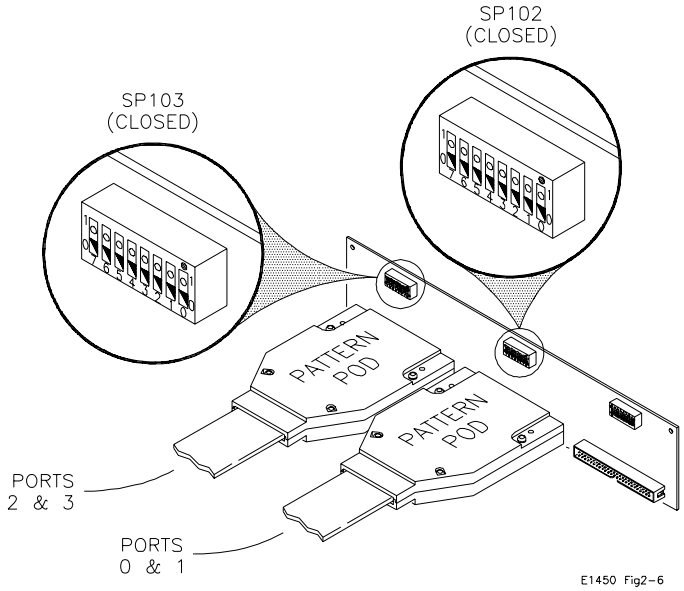

Figure 2-6. Test F-3: Comparing Patterns Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-3: Comparing Patterns"

Example Program

This program outputs a STIMulus pattern (55) via the selected STIMulus port of a Pattern I/O Module and an identical RESPonse pattern (55) via the selected RESPonse port of the module. The response pattern is then compared with the STIMulus pattern. If no errors occur, " " (the null string) is returned.

```
1       !Test F-3: Comparing Patterns
2       !
3       ! ---------------------------------------------- Initial Assignments ----------------------------------------------------
10      ASSIGN @Dft TO 70917                                        !Model D20 Address = 70917
20      DISP CHR$(129)                                              !Inverse video on display
30      CLEAR SCREEN
40      PRINT "Test F-3: Comparing Patterns"
50      PRINT
60      INPUT " How many Pattern I/O modules are installed? ",Mod   !Nbr of Pattern I/O modules
70  Retry_mod:      !
80      INPUT " Select module number (1,2,...) of Pattern I/O module   !Select  module to be tested
                to be tested ",Mod_no
90      IF Mod_no<1 OR Mod_no>Mod THEN
100       PRINT TABXY(1,16)," Invalid module number. Please reenter!Invalid module number warning
                                module number. "
110       BEEP
120       GOTO Retry_mod
130     END IF
140     CLEAR SCREEN
150 Retry_stim_port:     !
160     INPUT " Select STIMulus port number (0, 1, 2, or 3) ",Stim_port !Select STIMulus port number
170     IF Stim_port<0 OR Stim_port>3 THEN
180       PRINT TABXY(1,16),"Invalid STIMulus port number. Please   !Invalid STIMulus port number warning
                                reenter port number"
190       BEEP
200       GOTO Retry_stim_port
210     END IF
220     IF Stim_port=0 THEN Resp_port=1                             !STIM port 0, RESP port 1
230     IF Stim_port=1 THEN Resp_port=0                             !STIM port 1, RESP port 0
240     IF Stim_port=2 THEN Resp_port=3                             !STIM port 2, RESP port 3
250     IF Stim_port=3 THEN Resp_port=2                             !STIM port 3, RESP port 2
260     CLEAR SCREEN
261     ! ---------------------------------------- Set up Sequence ------------------------------------------------
270     Data_out$=","&"("&"@"&VAL$(Mod)&"("&VAL$(Stim_port)&"))"    !STIMulus port address
280     Data_in$=","&"("&"@"&VAL$(Mod)&"("&VAL$(Resp_port)&"))"     !RESPonse port address
```

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```
290  OUTPUT @Dft;"*RST"                                   !Set instrument to known condition
300  OUTPUT @Dft;"SEQ:DEL:ALL"                            !Delete all previous sequences
310  OUTPUT @Dft;"SEQ:DEF TEST_1,8"                       !Define seq "TEST_1" with 8 vectors
320  OUTPUT @Dft;"SEQ TEST_1"                             !Select "TEST_1" sequence
321  ! ---------------------------------- Set up STIMulus Group ----------------------------------------------
330  OUTPUT @Dft;"GRO:DEL:ALL"                            !Delete all previous pin groups
340  OUTPUT @Dft;"GRO:DEF DATA_OUT";Data_out$             !Define "DATA_OUT" group
350  OUTPUT @Dft;"GRO DATA_OUT"                           !Select group "DATA_OUT"
360  OUTPUT @Dft;"GRO:MODE STIM"                          !Set group to STIMulus mode
370  OUTPUT @Dft;"STIM:PATT:SEQ:REP 0,8,55"               !Load STIMulus pattern
380  OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                    !Use internal STIMulus clock 0
381  ! ---------------------------------- Set up RESPonse Group ----------------------------------------------
390  OUTPUT @Dft;"GRO:DEF DATA_IN";Data_in$               !Define "DATA_IN" pin group
400  OUTPUT @Dft;"GRO DATA_IN"                            !Select "DATA_IN" group
410  OUTPUT @Dft;"GRO:MODE RESP"                          !Set group to RESPonse mode
420  OUTPUT @Dft;"RESP:PATT:SEQ:REP 0,8,55"               !Load RESPonse pattern
430  OUTPUT @Dft;"RESP:CLOC:SOUR INT0"                    !Use internal RESPonse clock 0
440  OUTPUT @Dft;"RESP:COMP ON"                           !Enable comparison mode
441  !--------------------------- Set up Timing Cycle and Resolution ---------------------------------------
450  OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                       !Delete previous timing cycles
460  OUTPUT @Dft;"TIM:CYCL:DEF TC_1,750"                  !"TC_1" has 750 subcycles
470  OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,8,TC_1"              !Assign "TC_1" to each vector
480  OUTPUT @Dft;"TIM:RES MIN"                            !Each subcycle = 6.25 nsec
490  OUTPUT @Dft;"TIM:CYCL TC_1"                          !Select timing cycle "TC_1"
500  OUTPUT @Dft;"TIM:CYCL:RPCL0 3"                       !Delay RESPonse clock by 3 subcycles
510  CLEAR SCREEN
520  PRINT "1. Make sure that switches SP102 and SP103 are CLOSED."
530  PRINT
540  PRINT  "2. When this test is RUN, LEDs 0, 1, 2, 4, and 5 on"
550  PRINT  "   STIMulus port";Stim_port;"and on RESPonse port";Resp_port;"should"
560  PRINT  "light for 5 seconds and then turn OFF."
570  DISP " Press Continue when ready to observe the LEDs "
580  PAUSE
590  CLEAR SCREEN
600  OUTPUT @Dft;"RUN"                                    !RUN program
601  ! ---------------------------- Compare DATA_IN response pattern ------------------------------------
610  DIM A$[100]
620  CLEAR SCREEN
630  OUTPUT @Dft;"RESP:COMP:ERR?"                         !Compare patterns
640  ENTER @Dft;A$                                        !Enter comparison result
```

(continued on next page)

```
650  CLEAR SCREEN
651  ! ---------------------------------------------------------- Display Results ----------------------------------------------
660  PRINT "Test F-3: Comparing Patterns"
670  PRINT
680  PRINT "Expected result on RESPonse port";Resp_port;"= "  "  "  "  "
690  PRINT "   Actual result on RESPonse port";Resp_port;"= ";A$
700  PRINT
710  PRINT  "If the result is not " " "  ", make sure SP102 (ports 0 and 1)"
720  PRINT  "or switch SP103 (ports 2 and 3) is CLOSED. If not, CLOSE the switch"
730  PRINT  "and rerun the test."
740  WAIT 5
750  OUTPUT @Dft;"*RST"                                    !Reset  instrument
760  END
```

Typical Result If the STIMulus and RESPonse patterns are identical, " " (the null string) is displayed. If the patterns are not identical, an error message is displayed. A typical result for RESPonse port 2 with no errors is:

```
Test F-3: Comparing Patterns

Expected result on RESPonse port 2 = " "
   Actual result  on RESPonse port 2 = " "
```

Test F-4: Control Outputs

Description

This test checks CONTROL 0 through CONTROL 7 outputs. If the CONTROL LEDs on the Light Board light sequentially, from 0 through 7, the test passes. You can use this test to check the Timing Module CONTROL outputs.

Set up Equipment

- Turn mainframe power OFF
- Make Light Board connections (see Figure 2-7)
  (SP101, SP102, and SP103 switch settings don't matter)
- Turn mainframe power ON

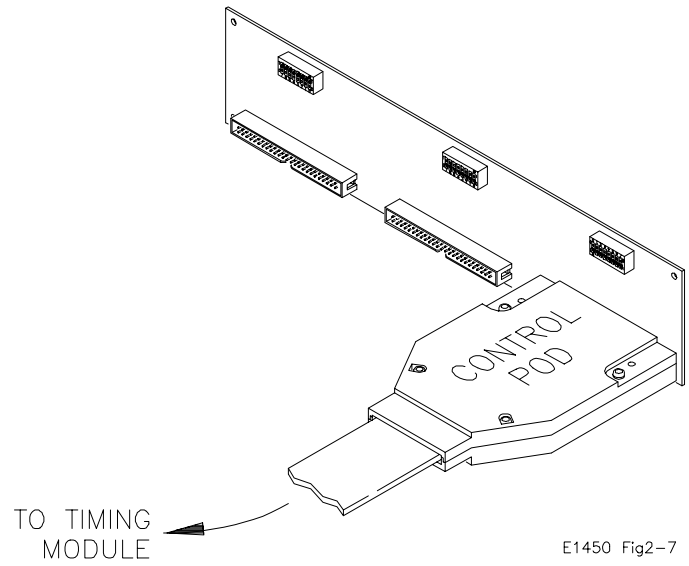


Figure 2-7. Test F-4: Control Outputs Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-4: Control Outputs"

Example Program This program generates a different waveform on each CONTROL outputs (CONTROL 0 through CONTROL 7). When the program is RUN, the CONTROL LEDs on the Light Board light sequentally (from 0 through 7) 10 times and then turn OFF.

```
1     !Test F-4: Control Outputs
2     !----------------------------------------------------Set up Sequence ----------------------------------------------
10    ASSIGN @Dft to 70917                                  !Model D20 address is 70917
20    OUTPUT @Dft;"*RST"                                    !Set instrument to known condition
30    OUTPUT @Dft;"SEQ:DEL:ALL"                             !Delete all previous sequences
40    OUTPUT @Dft;"SEQ:DEF TEST_1,10"                       !Sequence "TEST_1" has 10 vectors
50    OUTPUT @Dft;"SEQ TEST_1"                              !Select "TEST_1" sequence
51    !------------------------- Set up Timing Cycle and Resolution ----------------------------------------
60    OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                        !Delete all previous timing cycles
70    OUTPUT @Dft;"TIM:CYCL:DEF TC_1,1000"                  !Timing cycle "TC_1" has 1000
                                                            subcycles
80    OUTPUT @Dft;"TIM:RES 400E-6"                          !Each subcycle = 400 usec
81    !------------------------------------- Set up/enable Control outputs ---------------------------------
90    OUTPUT @Dft;"TIM:CYCL TC_1"                           !Select timing cycle "TC_1"
100   FOR I = 0 TO 7                                        !Loop to set up CONTROL outputs
110   OUTPUT @Dft;"TIM:CYCL:CONT"&VAL$(I)&":WAV 0, ";       !CONT0 goes HIGH @ 100 subcycles,
                  VAL$(100*(I+1))                           CONT1 @ 200, etc.
120   NEXT I
130   OUTPUT @Dft;"TIM:CONT ON"                             !Enable CONTROL outputs
131   !-------------------------------- RUN program, then disable CONTROL outputs ---------------------------------
140   PRINT "When this test is RUN, the CONTROL LEDs should light"
150   PRINT "sequentially from left to right 9 times, remain ON"
160   PRINT "for about 2 - 3 seconds and then turn OFF."
170   DISP " Press Continue when ready to observe the LEDs "
180   PAUSE
190   CLEAR SCREEN
200   OUTPUT @Dft;"RUN"                                     !RUN Model D20
210   WAIT 7                                                !All LEDs ON for 7 seconds
220   OUTPUT @Dft;"TIM:CONT OFF"                            !Disable control outputs; LEDs OFF
230   END
```

Typical Result When the program is RUN, the CONTROL LEDs on the Light Board light sequentally (from 0 through 7) 10 times and then turn OFF.

Test F-5: Trigger Test

Description

This test lights all CONTROL LEDs on the Light Board when a trigger from the selected source (see Table following) is input to the Timing Module.

Trigger Event	Trigger Source (TIM:TRIG:SOUR)
TTLTrg Trigger Bus Line 0	TTLT0
TTLTrg Trigger Bus Line 1	TTLT1
TTLTrg Trigger Bus Line 2	TTLT2
TTLTrg Trigger Bus Line 3	TTLT3
TTLTrg Trigger Bus Line 4	TTLT4
TTLTrg Trigger Bus Line 5	TTLT5
TTLTrg Trigger Bus Line 6	TTLT6
TTLTrg Trigger Bus Line 7	TTLT7
ECLTrg Trigger Bus Line 0	ECLT0
ECLTrg Trigger Bus Line 1	ECLT1
Timing Pod TRIGGER pin	EXT0
Timing Module TTL Trig In port	EXT1
Timing Module ECL Trig In port	EXT2
Trigger when *TRG issued	BUS
Trigger when COND3 = TRUE	EXT1

Set up Equipment

- Turn mainframe power OFF
- Make equipment connections (see Figure 2-8)
- Turn mainframe power ON

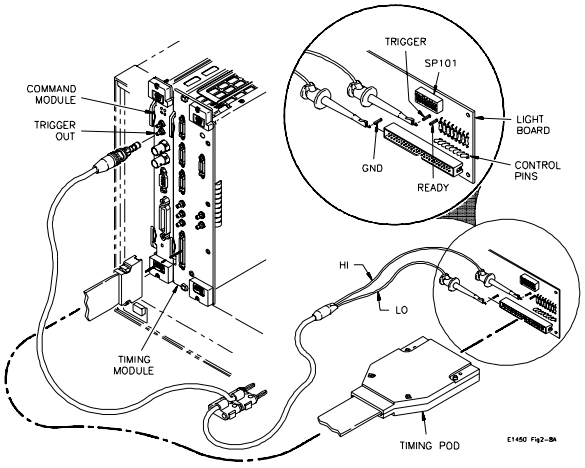
NOTE

For all trigger tests, disconnect any Pattern I/O Pods and connect a Timing Pod between the Timing Module and the Light Board. For trigger sources not shown in Figure 2-8, disconnect all other connections to the Command Module and Timing Module.

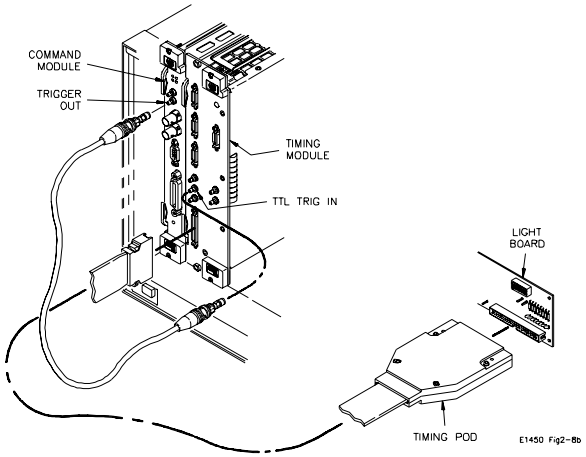
Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-5: Trigger Test"

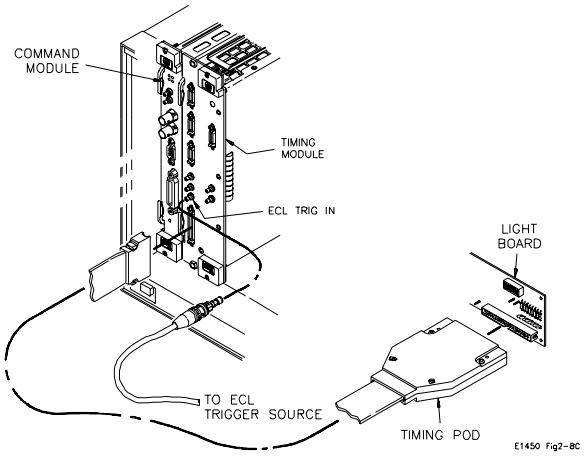
Case 10:
Timing Pod
TRIGGER line (EXT0)



Case 11:
TTL Trig In
Port (EXT1)



Case 12:
ECL Trig In
Port (EXT2)



Example Program This program lights CONTROL LEDs 0 through 7 on the Light Board when a trigger is generated from the trigger source selected. Available trigger input sources are listed in the Table under Description.

```
1    ! Test F-5: Trigger Test
2    !----------------------------------------------------Initial Setup ----------------------------------------------------
10   CLEAR SCREEN
20   PRINT "Test F-5: Trigger Test"
30   PRINT
40   PRINT "To begin this test:"
50   PRINT
60   PRINT "1. Disconnect all external sources from the Light Board."
70   PRINT
80   PRINT "2. Remove all Pattern I/O pods from the Light Board"
90   PRINT "   and from the installed Pattern I/O Modules."
100  PRINT
110  PRINT "3. Connect a Timing Pod from the Timing Module to the"
120  PRINT "   Light Board connector located below the CONTROL PINS."
130  DISP " Press Continue when ready "
140  PAUSE
150  CLEAR SCREEN
151     !------------------------------------ Select Trigger Source ----------------------------------------------------
160     ASSIGN @Dft TO 70917                                    !Model D20 address is 70917
170     ASSIGN @Cmd TO 70900                                    !Command Module address is 70900
180     OUTPUT @Cmd;"*RST"                                      !Set Command Module to known state
190     DIM Source$(0:14)[5]
200     DATA TTLT0, TTLT1, TTLT2, TTLT3, TTLT4, TTLT5, TTLT6,  !Read trigger source codes
TTLT7, ECLT0, ECLT1, EXT0, EXT1, EXT2, BUS, EXT1
210     READ Source$(*)
220     PRINT "Select a Trigger Source (Source in parentheses)"
230     PRINT
240     PRINT "   0 = TTL Trig 0  (TTLT0)"
250     PRINT "   1 = TTL Trig 1  (TTLT1)"
260     PRINT "   2 = TTL Trig 2  (TTLT2)"
270     PRINT "   3 = TTL Trig 3  (TTLT3)"
280     PRINT "   4 = TTL Trig 4  (TTLT4)"
290     PRINT "   5 = TTL Trig 5  (TTLT5)"
300     PRINT "   6 = TTL Trig 6  (TTLT6)"
310     PRINT "   7 = TTL Trig 7  (TTLT7)"
320     PRINT "   8 = ECL Trig 0  (ECLT0)"
330     PRINT "   9 = ECL Trig 1  (ECLT1)"
```

(continued on next page)

```
340    PRINT "  10 = Timing Pod TRIGGER line (EXT0)"
350    PRINT "  11 = Timing Module TTL Trig In port (EXT1)"
360    PRINT "  12 = Timing Module ECL Trig In port (EXT2)"
370    PRINT "  13 = Trigger when *TRG command is issued (BUS)"
380    PRINT "  14 = Trigger when qualifier COND3 = TRUE (EXT1)"
390 Retry:   !
400    INPUT " Enter the number (0 - 14) of the trigger source ",Trig_source
410    IF Trig_source<0 OR Trig_source>14 THEN
420        BEEP
430        PRINT
440        PRINT "Invalid number. Please reenter trigger source number."
450        GOTO Retry
460    END IF
470    CLEAR SCREEN
471     !----------------------------------------------------Set up Sequence
-------------------------------------------------------------
480    OUTPUT @Dft;"*RST"                                    !Set Model D20 to known state
490    OUTPUT @Dft;"SEQ:DEL:ALL"                             !Delete all previous sequences
500    OUTPUT @Dft;"SEQ:DEF TEST_1,8"                        !Seq "TEST_1" has 8 vectors
510    OUTPUT @Dft;"SEQ TEST_1"                              !Select "TEST_1"
511   !------------------------------ Set up Timing Cycle and Resolution ----------------------------------------------
520    OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                        !Delete all previous timing cycles
530    OUTPUT @Dft;"TIM:CYCL:DEF TC_1,900"                   !"TC_1" has 900 subcycles
540    OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,8,TC_1"               !Assign "TC_1" to each vector
550    OUTPUT @Dft;"TIM:RES 400E-6"                          !Each subcycle = 400 usec
551   !-----------------------------------------Set up Trigger Arming ------------------------------------------------------
560    OUTPUT @Dft;"TIM:CYCL TC_1"                           !Select timing cycle "TC_1"
570    OUTPUT @Dft;"TIM:ARM:SEQ:PART 0,1,0,0,0,0,0,0,0"      !Trigger required to generate
                                                             CONTROL outputs on vector 0
580    OUTPUT @Dft;"TIM:TRIG:SOUR ";Source$(Trig_source)     !Set Model D20 trigger source
590    FOR I=0 TO 7
600       OUTPUT @Dft;"TIM:CYCL:CONT"&VAL$(I)&":WAV 1"       !Enable CONTROL 0 - 7 outputs
                                                             for HIGH (ON)
610   NEXT I
620   OUTPUT @Dft;"TIM:CONT ON"                              !Enable CONTROL outputs
621   !---------------------------------- Issue Trigger from Source Selected ----------------------------------------
630   SELECT Trig_source                                     !Sel trigger according to source number
640   CASE <=9                                               !TTL and ECL trigger bus sources
```

(continued on next page)

```
641  !----------------------------------------TTL and ECL Bus Triggers ----------------------------------------------------
650    OUTPUT @Cmd:"OUTP:"&Source$(Trig_source)&":STAT ON"   !Set Command Module STATE ON
                                                              for sel trigger bus (TTLT or ECLT)
660    OUTPUT @Cmd:"OUTP:"&Source$(Trig_source)&":SOUR INT"  !Set Command Module trigger
                                                              source to INTernal
670    PRINT "Test for Trigger Source ";Source$(Trig_source)
680    PRINT
690    PRINT  "1. Disconnect all external sources from the Command"
700    PRINT  "   Module and from the Light Board."
710    PRINT
720    PRINT  "2. When the test if RUN, CONTROL LEDs 0 through 7"
730    PRINT  "    should light, remain ON for 5 seconds, then turn OFF."
740    DISP " Press Continue when ready to observe the LEDs "
750    PAUSE
760    CLEAR SCREEN
770    OUTPUT @Dft;"RUN"                                      !RUN Model D20
780    OUTPUT @Cmd:"OUTP:&Source$(Trig_source)&":IMM"         !Pulse the TTL or ECL trigger bus line
790  CASE =10                                                 !Light Board TRIGGER pin is source
791     ! ---------------------------------------- Light Board TRIGGER Pin ----------------------------------------------
800     PRINT "Trigger Test for ";Source$(Trig_source)
810     PRINT
820     PRINT "1. Connect cable HI lead from Command Module"
830     PRINT "    ""Trig Out"" port to TRIGGER pin on Light Board"
840     PRINT
850     PRINT "2. Connect cable LO lead from Command Module"
860     PRINT "    ""Trig Out"" port to GND pin on Light Board"
870     PRINT
880     PRINT "3. When this test is RUN, CONTROL LEDs 0 through 7"
890     PRINT "   should light, remain ON for 5 seconds, then turn OFF."
900     DISP " Make connections. Then, press Continue when ready to observe the LEDs. "
910     OUTPUT @Dft;"RUN"                                     !RUN Model D20
920    PAUSE
930    CLEAR SCREEN
940    OUTPUT @Cmd;"OUTP:EXT:STAT ON"                        !Enable Command Mod Trig Out port
950    OUTPUT @Cmd;"OUTP:EXT:SOUR NONE"                      !Set Trig Out  trigger source to NONE
960    OUTPUT @Cmd;"OUTP:EXT:IMM"                            !Output TTL pulse from Trig Out port
970  CASE =11                                                !TTL Trig In port
971     ! ---------------------------------- Timing Module TTL Trig In Port ----------------------------------------
980     OUTPUT @Cmd;"OUTP:EXT:STAT ON"                       !Enable Command Mod "Trig Out" port
990     OUTPUT @Cmd;"OUTP:EXT:SOUR NONE"                     !Set "Trig Out" port trigger source
```

(continued on next page)

```
1000    PRINT "Test for Trigger Source ";Source$(Trig_source)
1010    PRINT
1020    PRINT "1. Connect cable from Command Module ""Trig Out"""
1030    PRINT "   port to Timing Module ""TTL Trig In"" port"
1040    PRINT
1050    PRINT "2. When the test is RUN, CONTROL LEDs 0 through 7"
1060    PRINT "   should light, remain ON for 5 seconds, then turn OFF."
1070    DISP " Press Continue when ready to observe the LEDs "
1080    PAUSE
1090    CLEAR SCREEN
1100    OUTPUT @Dft;"RUN"                                   !RUN Model D20
1110    OUTPUT @Cmd;"OUTP:EXT:IMM"                          !Output TTL pulse from Command
                                                            Module "Trig Out" port
1120  CASE =12                                              !Timing Module ECL Trig In Port
1121    !---------------------------------- Timing Module ECL Trig In Port ----------------------------------------------
1130    PRINT "Trigger Test for ";Source$(Trig_source)
1140    PRINT
1150    PRINT "1. Connect cable from ECL trigger source"
1160    PRINT "   to Timing Module ""ECL Trig In"" port"
1170    DISP " Press Continue when connections are complete "
1180    PAUSE
1190    CLEAR SCREEN
1200    PRINT "When an ECL trigger is input, CONTROL LEDs 0 through 7"
1210    PRINT "    should light, remain ON for 5 seconds after you press"
1220    PRINT "Continue, then turn OFF."
1230    OUTPUT @Dft;"RUN"                                   !RUN Model D20
1240    DISP " Input ECL trigger from source. Then, press Continue. "
1250    PAUSE
1260    CLEAR SCREEN
1261    !--------------------------------GPIB Bus (*TRG) Triggering ----------------------------------------
1270  CASE =13
1280    PRINT  "Test for Trigger Source ";Source$(Trig_source)
1290    PRINT
1300    PRINT  "1. This part tests triggering when the *TRG command"
1310    PRINT  "   is issued"
1320    PRINT
1330    PRINT  "2. When the test is RUN, CONTROL LEDs 0 through 7"
1340    PRINT  "   should light, remain ON for 5 seconds, then turn OFF."
```

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```
1350    DISP " Press Continue when ready to observe the LEDs "
1360    PAUSE
1370    CLEAR SCREEN
1380    OUTPUT @Dft;"RUN"                                   !RUN Model D20
1390    OUTPUT @Dft;"*TRG"                                  !Generate *TRG command
1391    !----------------------------------Trigger When COND3 = TRUE ----------------------------------
1400  CASE =14                                              !Trigger when COND3 = T
1410    PRINT "Test for Trigger When COND3 = ( T ) (TRUE)"
1420    PRINT
1430    PRINT "1. This tests triggering when COND3 (Trigger Qualifier)"
1440    PRINT "   is set to ( T ) (TRUE). The trigger source is the front"
1450    PRINT "   panel TTL Trig In port (EXT1) and the trigger event is"
1460    PRINT "   a TTL pulse from the Command Module Trig Out port."
1470    PRINT
1480    PRINT "2. Connect a coaxial cable from the Command Module"
1490    PRINT "    ""Trig Out"" port to Timing Module ""TTL Trig In"" port."
1500    PRINT
1510    PRINT "3. When the test is RUN, CONTROL LEDs 0 through 7"
1520    PRINT "    should light, remain ON for 5 seconds, then turn OFF."
1530    DISP " Press Continue when ready to observe the LEDs "
1540    PAUSE
1550    CLEAR SCREEN
1560    OUTPUT @Cmd;"OUTP:EXT:STAT ON"                      !Enable Command Mod Trig Out port
1570    OUTPUT @Cmd;"OUTP:EXT:SOUR NONE"                    !Set Trig Out  trigger source to NONE
1580    OUTPUT @Dft;"STOP"                                  !STOP Model D20
1590    OUTPUT @Dft;"TIM:TRIG:QUAL ON"                      !Trigger event must occur when COND3
                                                            evals to TRUE for valid trigger
1600    OUTPUT @Dft;"TIM:COND3:DEF (T)"                     !Set COND3 ( T) (TRUE)
1610    WAIT .3                                             !Wait for settling
1620    OUTPUT @Dft;"RUN"                                   !RUN Model D20
1630    OUTPUT @Cmd;"OUTP:EXT:IMM"                          !Output TTL pulse from Command
                                                            Module Trig Out port
1640  END SELECT
1650  WAIT 5                                                !CONTROL LEDs ON for 5 seconds
1660  OUTPUT @Dft;"STOP"                                    !STOP Model D20
1670  OUTPUT @Dft;"TIM:CONT OFF"                            !Disable CONTROL outputs
1680  END
```

Typical Results When the program RUNs, connection instructions and "Press Continue" prompts appear. After you make the connections and press Continue (and input a trigger for the ECL source), all eight CONTROL LEDs on the Light Board should light for five seconds and then turn OFF.

Test F-6: Condition Inputs

Description

This test continues a sequence when COND0, COND1, or COND2 (as selected) evaluates to TRUE. You can use this test to check the COND0, COND1, and/or COND2 input function.

NOTE

COND3 is reserved for triggering. See "Test F-5: Trigger Test" for an example using COND3.

Set up Equipment

- Turn mainframe power OFF
- Make Light Board connections (see Figure 2-9)
- Turn mainframe power ON

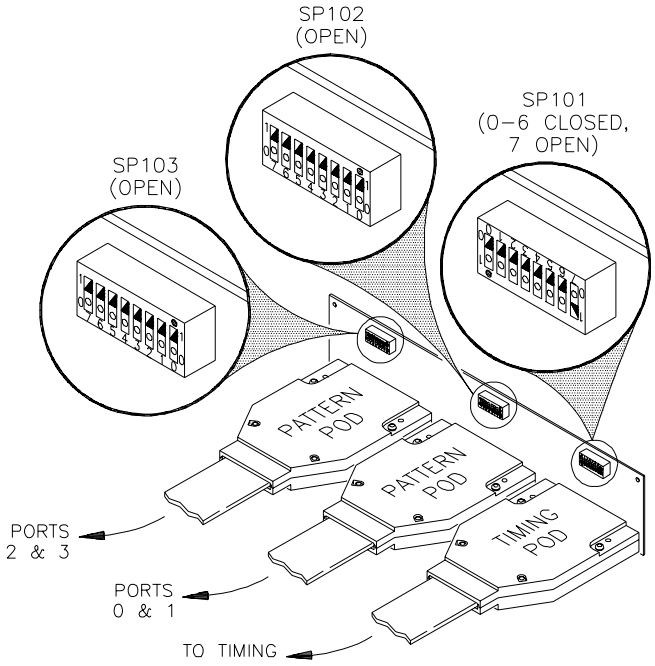

Figure 2-9. Test F-6: Condition Inputs Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-6: Condition Inputs"

Example Program

This program allows you to check the COND0, COND1, and/or COND2 Q (condition) inputs. The program uses the CONTROL outputs as CONDition inputs by connecting the CONTROL outputs to the CONDition inputs on the Light Board.

For this program, CONTROL outputs 0, 2, 4, and 6 are set HIGH and CONTROL outputs 1, 3, 5, and 7 are set LOW. When the Light Board switches on SP101 are CLOSED, and these CONTROL outputs are generated, the input to the Timing Module is the same as the boolean statement (Q0 AND NOT Q1 AND Q2 AND NOT Q3 AND Q4 AND NOT Q5 AND Q6 AND NOT Q7).

In this program, you select COND0, COND1, or COND2 as the Q condition to test. The instrument is then set for the above boolean statement for this condition. When the program is RUN, switch 7 on SP101 of the Light Board is OPEN and the sequence halts at vector 1 (LED 0 is ON), since the specified Q input condtion is not TRUE.

When switch 7 is closed, the specified Q input condition (Q0 AND NOT Q1 AND Q2 AND NOT Q3 AND Q4 AND NOT Q5 AND Q6 AND NOT Q7) is TRUE and the sequence advances through all vectors (LEDs 1 through 7 light).

```
1     !Test F-6: Condition Inputs
2     !
10    PRINT " Test F-6: Condition Inputs "
20    PRINT
30    INPUT " How many Pattern I/O modules are installed? ",Mods
40 Retry_mod: !
50    INPUT " Enter module number (1,2,...) of Pattern I/O module to be tested ",Mod_no
60    IF Mod_no <1 OR Mod_no >Mods THEN
70       BEEP
80       PRINT TABXY(1,15),"Invalid module number. Please reenter module number."
90       GOTO Retry_mod
100   END IF
110   CLEAR SCREEN
120 Retry_port: !
130   INPUT " Enter port number (0,1,2, or 3) to be tested ",Port_no
140   IF Port_no <0 OR Port_no >3 THEN
150      BEEP
160      PRINT TABXY(1,15),"Invalid port number. Please reenter port number."
```

(continued on next page)

```
170     GOTO Retry_port
180    END IF
190   CLEAR SCREEN
200  Retry_cond:    !
210   INPUT " Enter Q (CONDition) input to test (0, 1, or 2) ",Cond
220   IF Cond<0 OR Cond>2 THEN
230        BEEP
240        PRINT "Invalid number. Please reenter Q COND (0, 1, or 2)"
250       GOTO Retry_cond
260   END IF
270   CLEAR SCREEN
271   !----------------------------------------------Set up Sequence ----------------------------------------------
280   ASSIGN @Dft TO 70917                                    !Model D20 address is 70917
290   Number$=","&"("&"@"&VAL$(Mod_no)&"("&VAL$(Port_no)&"))"
300   OUTPUT @Dft;"*RST"                                      !Set instrument to known condition
310   OUTPUT @Dft;"SEQ:DEL:ALL"                               !Delete all previous sequences
320   OUTPUT @Dft;"SEQ:DEF TEST_1,9"                          !Sequence "TEST_1" has 9 vectors
330   OUTPUT @Dft;"SEQ TEST_1"                                !Select "TEST_1"
331   !------------------------------------------------- Define Pin Group ------------------------------------------------
340   OUTPUT @Dft;"GRO:DEL:ALL"
350   OUTPUT @Dft;"GRO:DEF DATA_OUT";Number$
360   OUTPUT @Dft;"GRO DATA OUT"
370   OUTPUT @Dft;"GRO:MODE STIM"
380   OUTPUT @Dft;"STIM:PATT:SEQ:PART 0,1,2,4,8,16,32,64,128,0"
390   OUTPUT @Dft;"STIM:CLOC:SOUR INT0"
391   !--------------------------------- Set up Timing Cycle and Resolution ---------------------------------------------
400   OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                          !Delete all previous timing cycles
410   OUTPUT @Dft;"TIM:CYCL:DEF TC_1,750"                     !Timing cycle "TC_1" has 750 subcycles
420   OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,9,TC_1"                 !Assign "TC_1" to all vectors
430   OUTPUT @Dft;"TIM:RES 400E-6"                            !Each subcycle = 400 usec
431   !---------------------------------------- Set up Condition Inputs ----------------------------------------------------
440   OUTPUT @Dft;"TIM:CYCL TC_1"                             !Select "TC_1"
450   OUTPUT @Dft;"TIM:COND"&VAL$(Cond)&":DEF (Q0 AND NOT Q1 AND Q2 AND NOT Q3 AND
Q4 AND NOT Q5 AND Q6 AND NOT Q7)"
460   OUTPUT @Dft;"TIM:CYCL:AWA:COND"&VAL$(Cond)&" 50,ON" !Cycle will wait until specified Q
                                                          (condition) is TRUE
470   OUTPUT @Dft;"TIM:CYCL:CONT0:WAV 1"
480   OUTPUT @Dft;"TIM:CYCL:CONT1:WAV 0"
490   OUTPUT @Dft;"TIM:CYCL:CONT2:WAV 1"
500   OUTPUT @Dft;"TIM:CYCL:CONT3:WAV 0"
```

```
510  OUTPUT @Dft;"TIM:CYCL:CONT4:WAV 1"
520  OUTPUT @Dft;"TIM:CYCL:CONT5:WAV 0"
530  OUTPUT @Dft;"TIM:CYCL:CONT6:WAV 1"
540  OUTPUT @Dft;"TIM:CYCL:CONT7:WAV 0"
541  !---------------------------------------- RUN program ----------------------------------------
550  PRINT "Starting the Sequence"
560  PRINT
570  PRINT "When this test is RUN, LED 0 of Port";Port_no;"should be ON"
580  PRINT "and the sequence should be halted at LED 0. Also, CONTROL"
590  PRINT "PINs LEDs 0, 2, 4, and 6 should be ON."
600  DISP "  Ensure switch 7 of SP101 is OPEN. Then, press Continue to start the sequence. "
610  PAUSE
620  CLEAR SCREEN
630  OUTPUT @Dft;"TIM:CONT ON"                    !Enable CONTROL outputs
640  OUTPUT @Dft;"RUN"                            !RUN Model D20
650  PRINT "Completing the Sequence"
660  PRINT
670  PRINT "To complete this sequence, CLOSE switch 7 of SP101 on the"
680  PRINT "Light Board. When switch 7 is CLOSED, the LEDs on Port";Port_no
690  PRINT "should light sequentially from 1 through 7 and CONTROL LEDs"
700  PRINT "0, 2, 4, and 6 should remain ON."
710  DISP " Close switch 7 of SP101. Then, press Continue to end this program. "
720  PAUSE
730  OUTPUT @Dft;"*RST"                           !Reset instrument
740  END
```

Typical Results

Assume Port 2 of the Pattern I/O Module under test was selected. Then, when the program first RUNS, Port 2 LED 0 and CONTROL LEDs 0, 2, 4, and 6 should turn ON. When switch 7 of SP101 is CLOSED, the sequence should advance from LED 1 through LED 7 on Port 2.

Test F-7: Marker Outputs

Description

This test has two parts: Part 1 generates pulses (markers) from the Timing Module front panel Marker Out SMB connector for selected vectors of the output sequence. Part 2 checks the Timing Module Marker Output drive of the TTLTrg bus lines (TTLT0 - TTLT7).

Set up Equipment

- Turn mainframe and oscilloscope power OFF
- Connect cable from Marker Out port to oscilloscope (see Figure 2-10)
- Turn mainframe and oscilloscope power ON
- Set up oscilloscope

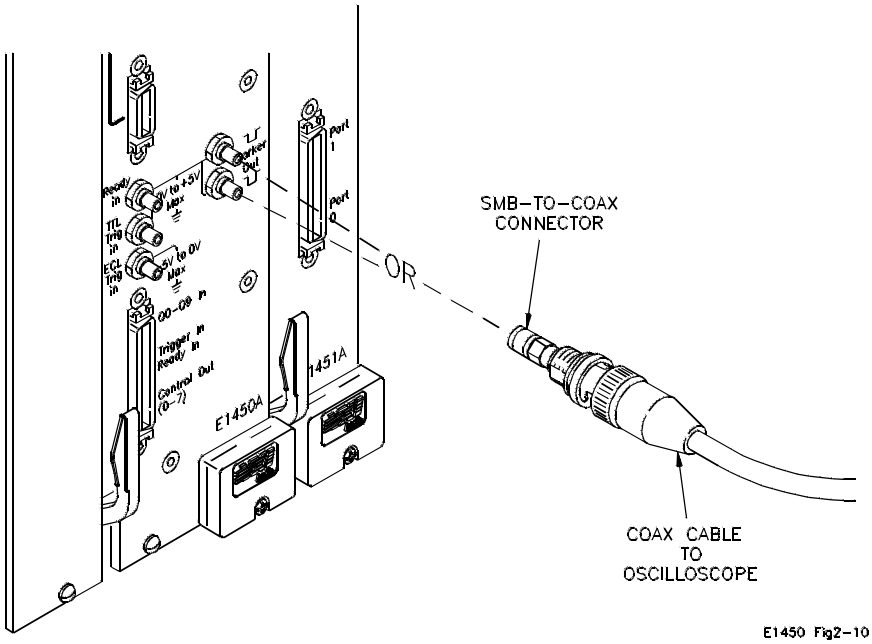

Figure 2-10. Marker Outputs Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-7: Marker Outputs"

Example Program

This program has two parts: Part 1 outputs a marker pulse from the Timing Module Marker Out port for each even-numbered vector in the DATA_OUT pin group pattern (vectors 2, 4, 6, and 8). Part 2 checks the Marker Out drive of the TTLTrg VXIbus lines (TTLT0 - TTLT7).

To test Part 2, the TTLTrg line you select (TTLT0 - TTLT7) is enabled with OUTP:TTLT<n>:STAT ON (line 590). For this program, each vector is 200 µsec long (20 subcycles @ 10 µsec per subcycle). Marker Outputs are generated at vectors 0, 2, 4, and 6 with TIM:MARK:SEQ:PART 0,1,0,1,0,1,0,1,0 (line 240). An await-for-trigger state is set for vectors 1, 3, 5, and 7 with TIM:ARM:SEQ:PART 0,0,1,0,1,0,1,0,1 (line 570). The trigger source is set with TIM:TRIG:SOUR (line 580), and a trigger delay of 300 µsec is set with TIM:TRIG:DEL 300E-6 (line 600).

For example, at t = 0 (see Figure 2-11) a Marker Output is generated for vector 0 and a TTLTrg 0 trigger is issued. Vector 0 lasts for 200 µsec and the trigger is delayed 300 µsec, so the TTLT0 trigger occurs at 300 µsec (during vector 1 execution). Since the instrument is set to the await-for-trigger state on vector 1, the sequence will not advance until the TTLT0 trigger is generated. The TTLT0 trigger, in turn, is driven by the Marker Out pulse.

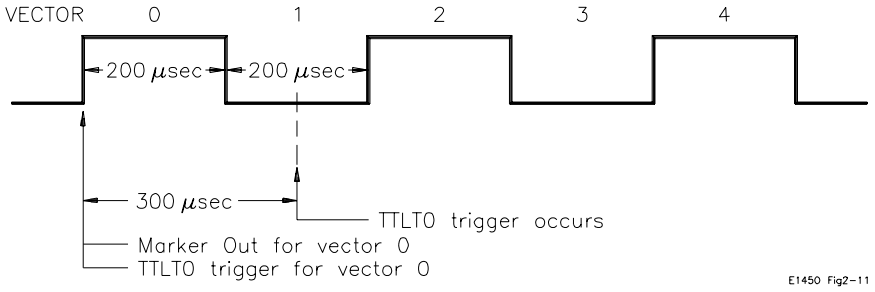

Figure 2-11. Example: Triggering TTLT0 with Marker Out

The sequence is monitored by querying the Status Operation Register. If the sequence completes successfully (all Marker Outputs and specified TTLTrg triggers occur), the Status Operation Register content = 256 (no errors). In this case, the program displays a TEST PASSED indication and lists the Status Operation Register contents.

If the sequence does not complete successfully, the instrument will halt and the Status Operation Register content = 32 (waiting for trigger). In this case, the program displays a TEST FAILED indication and lists the Status Operation Register contents.

```
1       !Test F_7: Marker Outputs
2     !---------------------------------------------------- Test Selection ----------------------------------------------------
10    CLEAR SCREEN
20    PRINT "Test F-7: Marker Outputs"
30    PRINT
40    PRINT "Marker Output Destination"
50    PRINT
60    PRINT "1 = Marker Output from Timing Module Marker Out port"
70    PRINT "2 = Marker Output to TTLT0 - TTLT7  backplane trigger bus"
80 Retry:    !
90    INPUT " Enter Marker Output Destination (1 or 2) ",Mark_outp    !Select Marker Out port or TTLTrg drive
100   IF Mark_outp<1 OR Mark_outp>2 THEN
110     PRINT TABXY(1,10),"Invalid number. Please reenter number for Marker Output Destination."
120     BEEP
130     GOTO Retry
140   END IF
141   !---------------------------------------------------- Set up Sequence ----------------------------------------------------
150   ASSIGN @Dft TO 70917                                    !Model D20 address is 70917
160   OUTPUT @Dft;"*RST"                                      !Set instrument to known condition
170   OUTPUT @Dft;"SEQ:DEL:ALL"                               !Delete all previous sequences
180   OUTPUT @Dft;"SEQ:DEF TEST_1,8"                          !Sequence "TEST_1" has 8 vectors
190   OUTPUT @Dft;"SEQ TEST_1"                                !Select "TEST_1"
191   !---------------------------------- Set up Timing Cycle and Resolution ----------------------------------------
200   OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                          !Delete all previous timing cycles
210   OUTPUT @Dft;"TIM:CYCL:DEF TC_1,20"                      !Timing cycle "TC_1" has 20 subcycles
220   OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,8,TC_1"                 !Assign "TC_1" to each subcycle
230   OUTPUT @Dft;"TIM:RES 10E-6"                             !Each subcycle = 10 usec
231   !---------------------------------------- Set up marker signal, run program ----------------------------------------
240   OUTPUT @Dft;"TIM:MARK:SEQ:PART 0,1,0,1,0,1,0,1,0"       !Enable Marker Out on vectors 1,3,5,
                                                              and 7
250   SELECT Mark_outp
260   CASE =1                                                 !Marker Output port to oscilloscope test
261   !---------------------------------- Part 1: Marker Out port to oscilloscope test ----------------------------------
270     CLEAR SCREEN
280     PRINT "Marker Output From ""Marker Out"" Port"
290     PRINT
300     PRINT "1. To observe the Marker Output pulses, set the oscilloscope"
310     PRINT "    to 200 usec/div timebase, 2.5V/div amplitude, and ""Awaiting"""
320     PRINT "    ""Trigger"" state (press SINGLE on Agilent 54503A SYSTEM CONTROL)."
330     PRINT
```

(continued on next page)

```
340   PRINT "2. As the test RUNs, the oscilloscope should display"
350   PRINT "    four Marker Output pulses with 200 usec pulse widths."
360   DISP " Press Continue when ready to observe the scope "
370   PAUSE
380   CLEAR SCREEN
390   OUTPUT @Dft;"RUN"                                    !RUN program
400   GOTO End_test                                        !End of Part 1
410 CASE =2                                                !TTLTrg bus lines test
411 !-------------------------- Part 2: Marker Output to TTLTrg lines test ----------------------------------------
420   CLEAR SCREEN
430   PRINT "Test F-7: Marker Outputs"
440   PRINT
450   PRINT "Marker Output to TTLT0 - TTLT7 Trigger Bus."
460   PRINT
470   PRINT "Disconnect cable if attached to Timing Module ""'Marker"""""
480   PRINT "Out port."
490 Retry1:  !
500   INPUT " Enter TTLT Trigger Bus Line to check (0 - 7) ",Bus   !Select TTLTrg bus (TTLT0 - TTLT7) to
                                                                   test
510   IF Bus<0 OR Bus>7 THEN
520     PRINT TABXY(1,10),"Invalid number. Please reenter number for Bus Line. "
530     BEEP
540     GOTO Retry1
550   END IF
560   CLEAR SCREEN
570   OUTPUT @Dft;"TIM:ARM:SEQ:PART 0,0,1,0,1,0,1,0,1"     !Set sequence to "await-for-trigger"
                                                           state on vectors 0,2,4, and 6
580   OUTPUT @Dft;"TIM:TRIG:SOUR TTLT"&VAL$(Bus)&""'       !Select trigger source (TTLT0 - TTLT7)
590   OUTPUT @Dft;"OUTP:TTLT"&VAL$(Bus)&":STAT ON"         !Enable configuration of sel trigger bus
600   OUTPUT @Dft;"TIM:TRIG:DEL 300E-6"                    !300 usec trigger delay
610   OUTPUT @Dft;"RUN"                                    !RUN program
620   WAIT 3
630   OUTPUT @Dft;"STAT:OPER:COND?"                        !Query Operation Status Register
640   ENTER @Dft;A                                         !Enter contents
650   IF BIT(A,5)=1 THEN                                   !Check bit 5 (waiting for trigger) state
660     PRINT "   Operation Status Register Contents =";A;"(Waiting for Trigger)"
670     PRINT "   Test for TTLT";Bus;"FAILED"              !Test FAILED indication
680   ELSE
690     PRINT "   Operation Status Register Contents =";A;"(No error)"
700     PRINT "   Test for TTLT";Bus;"PASSED"              !Test PASSED indication
```

(continued on next page)

```
710    END IF                                        !End Part 2 test
720  END SELECT
730 End_test:  !
740  END
```

Typical Results

Figure 2-12 shows a typical oscilloscope display for Marker Output pulses (Part 1 of the test). The display should show four pulses (vectors 0, 2, 4, and 6) with 200 µsec pulse widths.

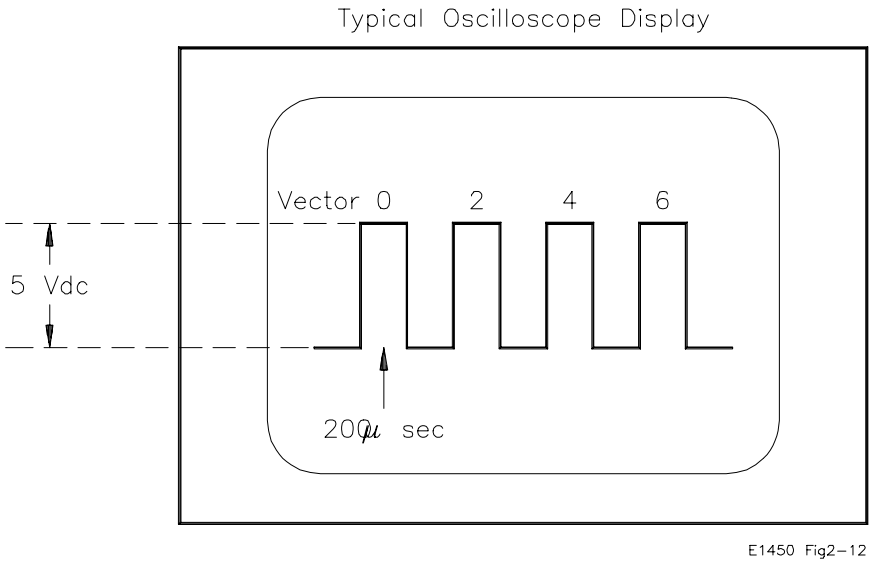

Figure 2-12. Typical Oscilloscope Display

Test F-8: End-If-Ready Inputs

Description

This test checks the End-If-Ready (EIR) function of the Model D20. Tests for two input sources are provided:

- The Timing Module Front Panel "Ready In" port
- The Light Board "READY" pin

Set up Equipment

- Turn mainframe power OFF
- Make equipment connections (see Figure 2-13)
- Turn mainframe power ON

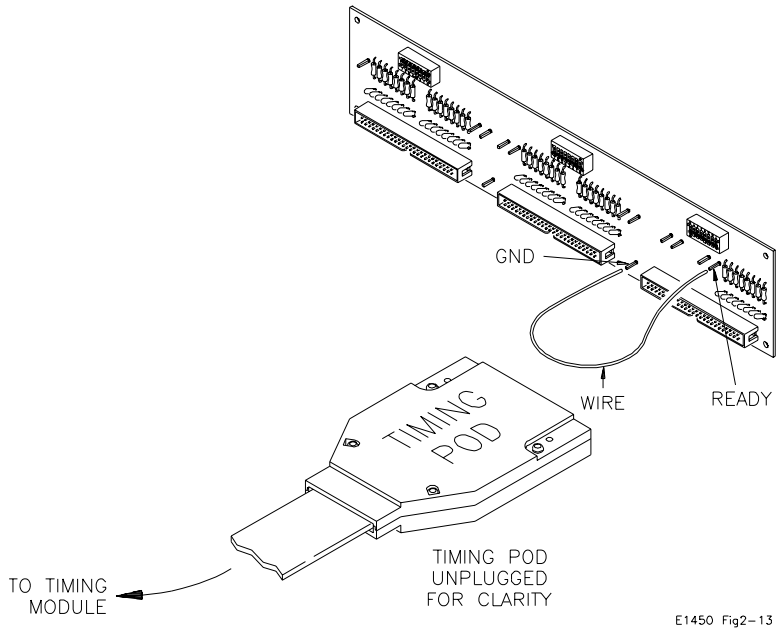

Figure 2-13. End-If-Ready Inputs Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-8: End-if-Ready Inputs"

Example Program

This example sequentially lights CONTROL LEDs on the Light Board. When the End-If-Ready signal is FALSE, CONTROL LEDs 0 through 7 light sequentially. When the End-If-Ready signal is TRUE, only CONTROL LEDs 0 through 3 light sequentially.

NOTE

When RUNning the example program using the Timing Module Front Panel Ready In port as the source, make sure the Light Board READY pin is NOT connected to the GND pin.

When running the program using the Light Board READY pin, make sure the 50 Ω SMB connecter is REMOVED from the Timing Module Ready In port.

```
1     ! Test F-8: End-If-Ready Inputs
2     !
3     ! ---------------------------------------- Address Assignments ----------------------------------------
10    ASSIGN @Dft TO 70917                          !Model D20 address is 70917
20    ASSIGN @Cmd TO 70900                          !Command Module address is 70900
21    !---------------------------------------- Set up Sequence ----------------------------------------
30    OUTPUT @Dft;"*RST"                            !Set Model D20 to known condition
40    OUTPUT @Dft;"SEQ:DEL:ALL"                     !Delete all existing sequences
50    OUTPUT @Dft;"SEQ:DEF TEST_1,8"                !Sequence "TEST_1" has 8 vectors
60    OUTPUT @Dft;"SEQ TEST_1"                      !Select "TEST_1"
61    !------------------------------------ Set up Timing Cycle and Resolution ------------------------------------
70    OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                !Delete all previous timing cycles
80    OUTPUT @Dft;"TIM:CYCL:DEF TC_1,1000"          !Timing cycle "TC_1" has 1000
                                                    subcycles
90    OUTPUT @Dft;"TIM:RES 400E-6"                  !Each subcycle = 400 usec
100   OUTPUT @Dft;"TIM:CYCL TC_1"                   !Select timing cycle "TC_1"
110   OUTPUT @Dft;"TIM:CYCL:REP 0,8,TC_1"           !Assign "TC_1" to all vectors
120   OUTPUT @Dft;"TIM:ARM:SEQ:REP 0,8,0"           !Disarms all vectors
130   FOR I=0 TO 7
140     OUTPUT @Dft;"TIM:CYCL:CONT"&VAL$(I)&":WAV 0, ";
                    VAL$(100*(I+1))                 !CONTROL 0 goes HIGH at 100
                                                    subcycles, CONTROL 1 at 200
                                                    subcycles, etc.
150   NEXT I
160   OUTPUT @Dft;"TIM:CONT ON"                     !Enable CONTROL outputs
170   OUTPUT @Dft;"TIM:CYCL:EIR 400,1"              !Set End-If-Ready point at 400 subcycles
171   !-------------------------------------Select End-If-Ready Input Source-------------------------------------
180   PRINT "Select End-If-Ready Input Source"
190   PRINT
200   PRINT "1 = Timing Module Front Panel ""Ready In"" port"
210   PRINT "2 = Light Board ""READY"" pin"
220 Retry_source:   !
```

(continued on next page)

```
230  INPUT " Select End-If-Ready Source (1 or 2) ",Source
240  IF Source<1 OR Source>2 THEN
250    PRINT TABXY(1,7),"Incorrect entry. Please reenter source number (1 or 2)"
260    BEEP
270    GOTO Retry_source
280  END IF
290  CLEAR SCREEN
300  SELECT Source
310  CASE =1                                          !EIR source is Timing Module
                                                      Ready In port
311  !-----------------------------------Timing Module Ready In Port ----------------------------------------------
320    Flag1=0
330    PRINT "Timing Module ""Ready In"" port: Ready-In FALSE test"
340    PRINT
350    PRINT  "1. Connect a Timing Pod from the Light Board CONTROL PIN"
360    PRINT  "    connectors to the Timing Module. Disconnect all"
370    PRINT  "    Pattern I/O Pods from the Light Board."
380    PRINT
390    PRINT "   2. Connect a coaxial cable from the Command Module ""Trig Out"""
400    PRINT "       port to the ""Ready In"" port on the Timing Module (use an"
410    PRINT "       SMB-to-coax adaptor to connect to the ""Ready-In"" port)."
420    PRINT
430    PRINT "   3. Make sure the Light Board READY pin is NOT connected"
440    PRINT "       to the GND pin."
450    PRINT
460    PRINT "   4. When this test is RUN, the Ready In port input is set FALSE,"
470    PRINT "       so the timing cycle completes the full 1000 subcycles."
480    PRINT
490    PRINT "    5. For this part of the test, CONTROL LEDs 0 through 7 should"
500    PRINT "        light sequentially and the sequence should repeat 8 times."
510    DISP " Press Continue when ready to observe the LEDs "
520    PAUSE
530    CLEAR SCREEN
540 Rerun1:   !
550    OUTPUT @Cmd;"OUTP:EXT:STAT ON"                !Enable Command Mod Trig Out port
560    OUTPUT @Cmd;"OUTP:EXT:SOUR INT"               !Set Trig Out port trig source to
                                                     INTernal
570    OUTPUT @Cmd;"OUTP:EXT:LEV ";1-Flag1           !Output LEV 1 on first pass, LEV 0 on
                                                     second pass
580    OUTPUT @Dft;"RUN"                             !RUN program
590    Flag1=Flag1+1
600    WAIT 5
```

(continued on next page)

```
610    OUTPUT @Dft;"TIM:CONT OFF"                          !Disable CONTROL outputs
620    IF Flag1>1 THEN GOTO End_test
630    DISP  " Press Continue for Ready In port TRUE test "
640    PAUSE
650    CLEAR SCREEN
660    PRINT "Timing Module ""Ready In"" port: Ready-In TRUE test"
670    PRINT
680    PRINT "   1. For this part of the test, the Ready In port input is"
690    PRINT "       set TRUE, so the timing cycle ends after 400 subcycles."
700    PRINT
710    PRINT "   2. When this test is RUN, CONTROL LEDs 0 through 3 should"
720    PRINT "       light sequentially and the sequence should repeat 8 times."
730    DISP " Press Continue when ready to observe the LEDs "
740    PAUSE
750   OUTPUT @Dft;"TIM:CONT ON"                            !Enable CONTROL outputs
760    IF Flag1=1 THEN GOTO Rerun1
770   CASE =2                                              !Light Board READY pin is EIR source
771   ! ---------------------------------------- Light Board READY pin ----------------------------------------------
780     Flag2=0
790     PRINT "Light Board ""READY"" pin - Ready-In FALSE test"
800     PRINT
810     PRINT "    1. Connect a Timing Pod from the Light Board CONTROL PIN"
820     PRINT "        connectors to the Timing Module. Disconnect all"
830     PRINT "        Pattern I/O Pods from the Light Board."
840     PRINT
850     PRINT "   2.  Connect a wire between the READY pin and the GND pin on"
860     PRINT "        the Light Board. This sets the ""Ready In"" input FALSE,"
870     PRINT "       so the timing cycle completes the full 1000 subcycles."
880     PRINT
890     PRINT "   3.  When this test is RUN, CONTROL LEDs 0 through 7 should"
900     PRINT "        light sequentially and the sequence should repeat 8 times."
910     DISP " Press Continue when ready to observe the LEDs "
920     PAUSE
930     CLEAR SCREEN
940 Rerun:   !
950     OUTPUT @Dft;"RUN"                                   !RUN program
960     WAIT 5
970     OUTPUT @Dft;"TIM:CONT OFF"                          !Disable CONTROL outputs
990     Flag2=Flag2+1
990     IF Flag2>1 THEN GOTO End_test
```

(continued on next page)

```
1000    DISP   " Press Continue for Light Board Ready-In TRUE test "
1010    PAUSE
1020    CLEAR SCREEN
1030    PRINT "Light Board ""READY"" pin - Ready-In TRUE test"
1040    PRINT
1050    PRINT "   1. Remove the wire between the READY pin and the GND pin on"
1060    PRINT "      the Light Board. This sets the ""Ready-In"" input TRUE,"
1070    PRINT "      so the timing cycle ends after 400 subcycles."
1080    PRINT
1090    PRINT "   2. When this test is RUN, CONTROL LEDs 0 through 3 should"
1100    PRINT "      light sequentially and the sequence should repeat 8 times."
1110    DISP " Press Continue when ready to observe the LEDs "
1120    PAUSE
1130    CLEAR SCREEN
1140    OUTPUT @Dft;"TIM:CONT ON"                    !Enable CONTROL outputs
1150    IF Flag2=1 THEN GOTO Rerun
1160    END SELECT
1170  End_test:  !
1180    CLEAR SCREEN
1190    OUTPUT @Dft;"*RST"                           !Set Model D20 to known state
1200   END
```

Typical Results When the End-If-Ready input signal is FALSE, CONTROL LEDs 0 through 7 light sequentially. When the End-If-Ready input signal is TRUE, only CONTROL LEDs 0 through 3 light sequentially.

Test F-9: Clock Outputs

Description

This test verifies correct operation of the six STIMulus clocks (0 - 5) and the six RESPonse clocks (0 - 5). It also verifies that the Timing Module is properly generating all 12 clocks at maximum speed.

Set up Equipment

- Turn Mainframe Power OFF
- Disconnect ALL pods from Pattern I/O Modules
- Disconnect Timing Pod from Timing Module
- Remove Agilent E1452A Terminating Pattern I/O Module

- Remove ALL Agilent E1451A Pattern I/O Modules
- Set Agilent E1452A Module address for slot 1
- Install Agilent E1452A Module in slot 1 (see Figure 2-14)
- Turn Mainframe power ON

NOTE

If desired, you can rerun the test with Pattern I/O Modules and a Terminating Pattern I/O Module installed. Be sure to set the address switches correctly for each configuration. Pods are not required for this test.

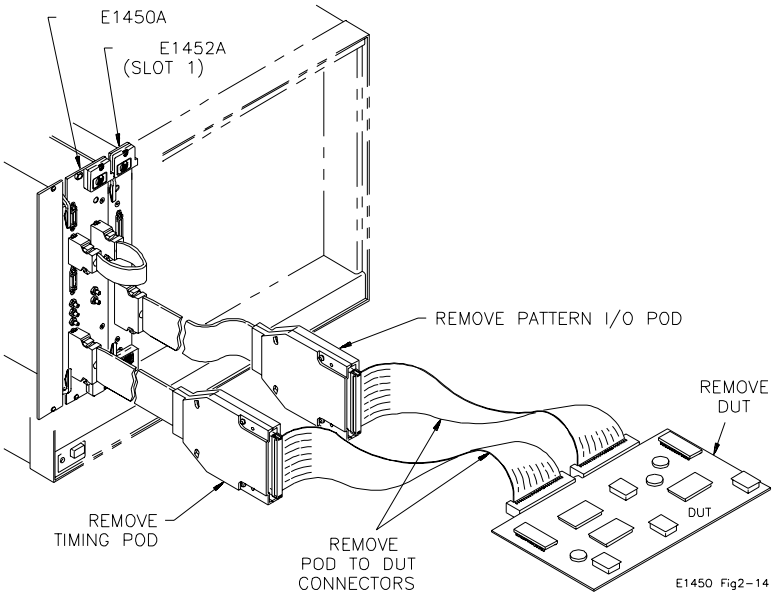

Figure 2-14. Clock Outputs Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "FUNC_VER"
- Press RUN
- Select "Test F-9: Clock Outputs"

Example Program

This program tests the six STIMulus Clocks (0 through 5) and the six RESPonse Clocks (0 through 5). For this test, Pattern I/O Module ports 0 and 1 are STIMulus ports and ports 2 and 3 are RESPonse ports. The program makes three tests.

The first test checks STIMulus/RESPonse clocks 0 and 1, the second test checks STIMulus/RESPonse clocks 2 and 3, and the third test checks STIMulus/RESPonse clocks 4 and 5.

Each test checks the contents of the Sequence Memory Address registers for ports 0 through 3. If the return for (STIMulus) ports 0 and 1 is "+10" and the return for (RESPonse) ports 2 and 3 is "+9", the test passes.

```
1   !Test F_9: Clock Outputs
2   !
10  PRINT "Test F-9: Clock Outputs"
11  !---------------------------------------------------- Set up Sequence ----------------------------------------------
20  ASSIGN @Dft TO 70917                                  !Model D20 address is 70917
30  OUTPUT @Dft;"*RST"                                    !Set instrument to known state
40  OUTPUT @Dft;"SEQ:DEL:ALL"                             !Delete all previous sequences
50  OUTPUT @Dft;"SEQ:DEF TEST_1,9"                        !Sequence "TEST_1" has 9 vectors
60  OUTPUT @Dft;"SEQ TEST_1"                              !Select "TEST_1"
61  ! ---------------------------------- Define STIMulus/RESPonse Groups ---------------------------------
70  OUTPUT @Dft;"GRO:DEL:ALL"                             !Delete all previous pin groups
80  OUTPUT @Dft;"GRO:DEF port_0,(@1(0))"                  !"port_0" group = port 0
90  OUTPUT @Dft;"GRO:DEF port_1,(@1(1))"                  !"port_1" group = port 1
100 OUTPUT @Dft;"GRO:DEF port_2,(@1(2))"                  !"port_2" group = port 2
110 OUTPUT @Dft;"GRO:DEF port_3,(@1(3))"                  !"port_3" group = port 3
111 !------------------------------------- Set up STIMulus Patterns ------------------------------------------
120 OUTPUT @Dft;"GRO port_0"                              !Select group "port_0"
130 OUTPUT @Dft;"GRO:MODE STIM"                           !Set group to STIMulus mode
140 OUTPUT @Dft;"STIM:PATT:SEQ:REP 0,9,0"                 !"port_0" STIMulus pattern = all 0s
150 OUTPUT @Dft;"GRO port_1"                              !Select group "port_1"
160 OUTPUT @Dft;"GRO:MODE STIM"                           !Set group to STIMulus mode
170 OUTPUT @Dft;"STIM:PATT:SEQ:REP 0,9,0"                 !"port_1" STIMulus pattern = all 0s
```

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```
171 !-------------------------------------- Set up Timing Cycle and Resolution ------------------------------
180 OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                    !Delete all previous timing cycles
190 OUTPUT @Dft;"TIM:CYCL:DEF TC_1,9"                 !Timing cycle "TC_1" has 9 subcycles
200 OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,9,TC_1"           !Assign "TC_1" to each vector
201 !---------------------------------- Check STIMulus and RESPonse Clocks 0/1 -------------------------
210 OUTPUT @Dft;"GRO port_0"                          !Select "port_0" group
220 OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                 !Use STIMulus clock 0
230 OUTPUT @Dft;"GRO port_1"                          !Select "port_1" group
240 OUTPUT @Dft;"STIM:CLOC:SOUR INT1"                 !Use STIMulus clock 1
250 OUTPUT @Dft;"GRO port_2"                          !Select "port_2" group
260 OUTPUT @Dft;"GRO:MODE RESP"                       !Set group to RESPonse mode
270 OUTPUT @Dft;"RESP:CLOC:SOUR INT0"                 !Use RESPonse clock 0
280 OUTPUT @Dft;"GRO port_3"                          !Select "port_3" group
290 OUTPUT @Dft;"GRO:MODE RESP"                       !Set group to RESPonse mode
300 OUTPUT @Dft;"RESP:CLOC:SOUR INT1"                 !Use RESPonse clock 1
310 CALL Clk_test(@Dft,1)                             !Call Clk_test to test clocks 0,1
311 ! ---------------------------------- Check STIMulus and RESPonse Clocks 2/3 -------------------------
320 OUTPUT @Dft;"GRO port_0"                          !Select group "port_0"
330 OUTPUT @Dft;"STIM:CLOC:SOUR INT2"                 !Use STIMulus clock 2
340 OUTPUT @Dft;"GRO port_1"                          !Select group "port_1"
350 OUTPUT @Dft;"STIM:CLOC:SOUR INT3"                 !Use STIMulus clock 3
360 OUTPUT @Dft;"GRO port_2"                          !Select group "port_2"
370 OUTPUT @Dft;"RESP:CLOC:SOUR INT2"                 !Use RESPonse clock 2
380 OUTPUT @Dft;"GRO port_3"                          !Select group "port_3"
390 OUTPUT @Dft;"RESP:CLOC:SOUR INT3"                 !Use RESPonse clock 3
400 CALL Clk_test(@Dft,2)                             !Call Clk_test to test clocks 2,3
401 !---------------------------------- Check STIMulus and RESPonse Clocks 4/5 -------------------------
410 OUTPUT @Dft;"GRO port_0"                          !Select group "port_0"
420 OUTPUT @Dft;"STIM:CLOC:SOUR INT4"                 !Use STIMulus clock 4
430 OUTPUT @Dft;"GRO port_1"                          !Select group "port_1"
440 OUTPUT @Dft;"STIM:CLOC:SOUR INT5"                 !Use STIMulus clock 5
450 OUTPUT @Dft;"GRO port_2"                          !Select group "port_2"
460 OUTPUT @Dft;"RESP:CLOC:SOUR INT4"                 !Use RESPonse clock 4
470 OUTPUT @Dft;"GRO port_3"                          !Select group "port_3"
480 OUTPUT @Dft;"RESP:CLOC:SOUR INT5"                 !Use RESPonse clock 5
490 CALL Clk_test(@Dft,3)                             !Call Clk_test to test clocks 4,5
500 PRINT
510 PRINT "********** CLOCK TEST PASSED ***********"
520 END
```

(continued on next page)

```
530  SUB Clk_test(@Dft,Flag)                                    !Query clock test results
531  ! ---------------------------------- Query STIMulus/RESPonse Clock Results ----------------------
540    DIM String$(3)[4],A(3)
550    OUTPUT @Dft;"RUN;*WAI"                                   !RUN program
560    FOR I=0 TO 3                                             !Loop to check register for ports 0 - 3
570      OUTPUT @Dft;":DIAG:REG? 1, ";VAL$(8+14*I)              !Query Seq Memory Addr registers
580      ENTER @Dft;String$(I)                                  !Enter result
590      A(I)=VAL(String$(I))                                   !Equivalent numeric value
600      IF (I=0 OR I=1) AND A(I)<>10 THEN CALL Fail(@Dft,I,Flag)  !If STIM clock <>+10, test fails
610      IF (I=2 OR I=3) AND A(I)<>9 THEN CALL Fail(@Dft,I,Flag)   !If RESP clock <>+9, test fails
620    NEXT I
630  SUBEND
640  SUB Fail(@Dft,I,Flag)                                      !Clock failure indication
641  ! ------------------------------------- Clock Failure Indication ------------------------------------------------
650    DIM Clock$(11)[10]
660    DATA STIMulus 0,STIMulus 1,RESPonse 0,RESPonse 1
670    DATA STIMulus 2,STIMulus 3,RESPonse 2,RESPonse 3
680    DATA STIMulus 4,STIMulus 5,RESPonse 4,RESPonse 5
690    READ Clock$(*)                                           !Enter clock identification data
700    IF Flag=1 THEN Clock$(I)=Clock$(I)                       !Identification for clocks 0,1
710    IF Flag=2 THEN Clock$(I)=Clock$(I+4)                     !Identification for clocks 2,3
720    IF Flag=3 THEN Clock$(I)=Clock$(I+8)                     !Identification for clocks 4,5
730    PRINT
740    PRINT "********* CLOCK TEST FAILED ************"
750    PRINT
760    PRINT "First FAILED Clock Detected = ";Clock$(I)
770    STOP
780  SUBEND
```

Typical Results

If the test passes, **********CLOCK TEST PASSED ********** is displayed. If the test fails for any clock ****** CLOCK TEST FAILED ********* and the first failed clock detected is displayed.
For example, if STIMulus Clock 0 failed, the display is:

Test F-9: Clock Outputs

********** CLOCK TEST FAILED **********

First FAILED Clock Detected = STIMulus 0

Performance Verification Tests

Performance verification test objectives are to instill a high degree of confidence that the Agilent 75000 Model D20 Digital Functional Test System is meeting the specifications listed in *Appendix A - Specifications* of the *Model D20 Task and Command Reference*. The performance verification tests are:

- Test P-1: Subcycle Period Accuracy
- Test P-2: System Skew Accuracy

Test P-1: Subcycle Period Accuracy

Description

This test verifies the accuracy of the subcycle period. A timing cycle of 20 subcycles @6.25 nsec per subcycle is defined and specified for five vectors. A marker output is generated by the DIAG:SEQ:LOOP command on each loop through the five vectors. The resulting frequency of the marker output is 1.6 MHz ±0.0001 MHz (total period = 6.25 nsec per subcycle period x 20 subcycles per timing cycle x 5 timing cycles per sequence = 625 nsec ±0.01%).

Set up Equipment

- Connect the MARKER output to the Counter (see Figure 2-15).

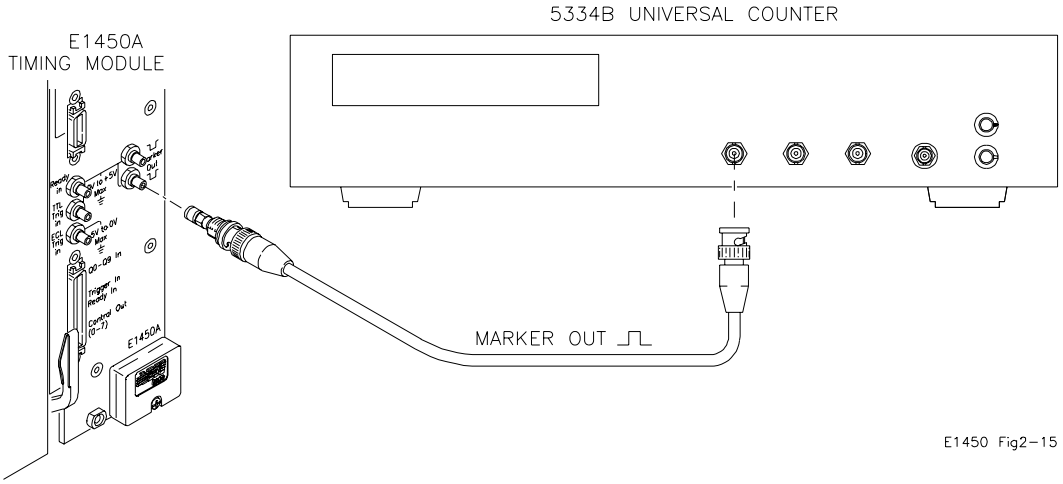

Figure 2-15. Subcycle Period Accuracy Test Connections

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "PERF_VER"
- Press RUN
- Select "Test P-1: Subcycle Period Accuracy"

Example Program This program sets up five vectors and a timing cycle of 20 subcycles. The five vectors are looped continuously using the DIAGnostic:SEQuence:LOOP command to provide a marker output at the end of each loop.

```
1   ! Test P-1: Subcycle Period Accuracy
2   !
10  CLEAR SCREEN
20  Addr=70917                                          !70917 is default address
30  INPUT " Enter Model D20 address (70917 is default) ",Addr
40  ASSIGN @Dft TO Addr                                 !Assign address to Model D20
50  CLEAR SCREEN
60  PRINT "Read the frequency displayed on the frequency counter."
70  PRINT "The frequency should be between 1.5999 MHz and 1.6001 MHz."
80  OUTPUT @Dft;"*RST"                                  !Set instrument to known condition
90  OUTPUT @Dft;"SEQ:DEL:ALL"                           !Delete all previous sequences
100 OUTPUT @Dft;"SEQ:DEF TEST_1,5"                      !Sequence "TEST_1" has 5 vectors
110 OUTPUT @Dft;"SEQ TEST_1"                            !Select "TEST_1"
120 OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                      !Delete all timing cycles
130 OUTPUT @Dft;"TIM:CYCL:DEF TC_1,20"                  !Timing cycle "TC_1" has 20 subcycles
140 OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,5,TC_1"             !Assign "TC_1" to all vectors
150 OUTPUT @Dft;"TIM:RES MIN"                           !Each subcycle = 6.25 nsec
160 OUTPUT @Dft;"TIM:MARK:SEQ:PART 0,0,0,0,0,0"         !Disables marker out for all vectors
170 OUTPUT @Dft;"DIAG:SEQ:LOOP ON"                      !Enable looping
180 OUTPUT @Dft;"RUN"                                   !RUN program
190 DISP " Record result as desired. Then, press Continue."
200 PAUSE
210 CLEAR SCREEN
220 OUTPUT @Dft;"*RST"                                  !Reset instrument
230 END
```

Typical Results

The counter should read 1.6000 MHz ±0.0001 MHz (between 1.5999 MHz and 1.6001 MHz).

Test P-2: System Skew Accuracy

Description

This test provides a method to use an oscilloscope to manually measure skew on STIMulus pins. (Skew cannot be measured manually for RESPonse pins since a RESPonse event cannot be seen.) For this test, rising and falling signal skew are measured with respect to the port 0, pin 0 output on the selected Pattern I/O Module.

Skew is the unintentional time interval among two or more pin output-transition-events (STIMulus) or input-sample-events (RESPonse). Skew is seen as the horizontal displacement of threshold voltage crossings from simultaneous signal changes (as observed on an oscilloscope).

The threshold voltage for defining Model D20 skew is +1.6V. Figure 2-16 shows rising and falling signal skew (the time difference between the first signal crossing the threshold and the last signal crossing the threshold).

Set up Equipment

- Connect one scope probe to port 0, pin 0 on the Agilent E1454A

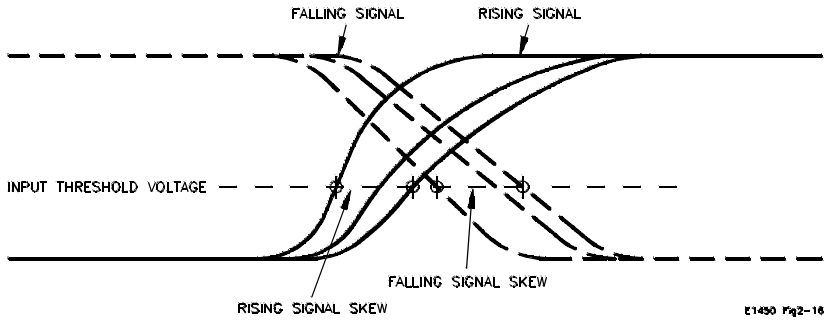

Figure 2-16. Rising and Falling Signal Skew

- Connect the second scope probe to port 0, pin 1 (see Figure 2-18).
- For measurements on other pins, move the second scope probe to the pin to be measured (leave the first scope probe connected to port 0, pin 0).

CAUTION

The oscilloscope probes CAN be connected directly to the pins on the Agilent E1451A or E1452A Pattern I/O Modules and to the CONTROL pins on the Agilent E1450A Timing Module. However, touching certain pins on these modules can cause module failure. See the *Agilent E1450 Hardware Manual and the Agilent E1451/1452 Hardware Manual* for information BEFORE touching the probe to the module connectors.

NOTE

See Figure 2-17 to build probe adaptors that make measuring signals at the pod much easier. If you use prebuilt probe adapters, connect the prebuilt probe adaptors to the oscilloscope probes.

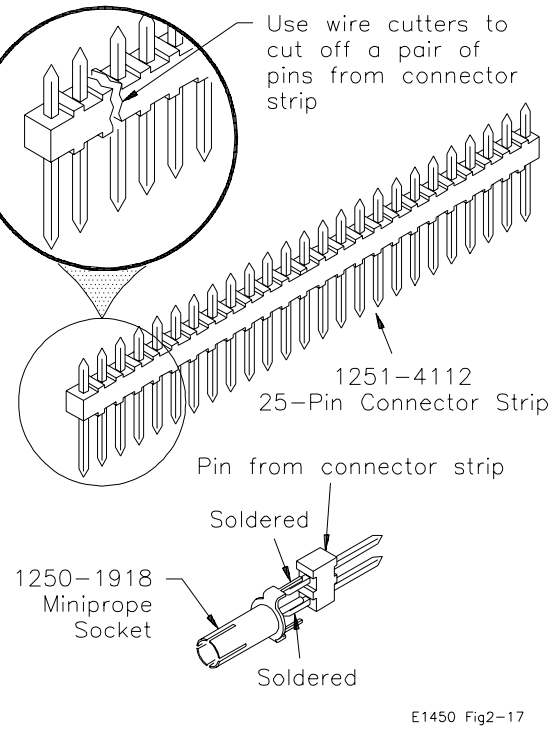

Figure 2-17. Probe Adapter for Measuring Skew

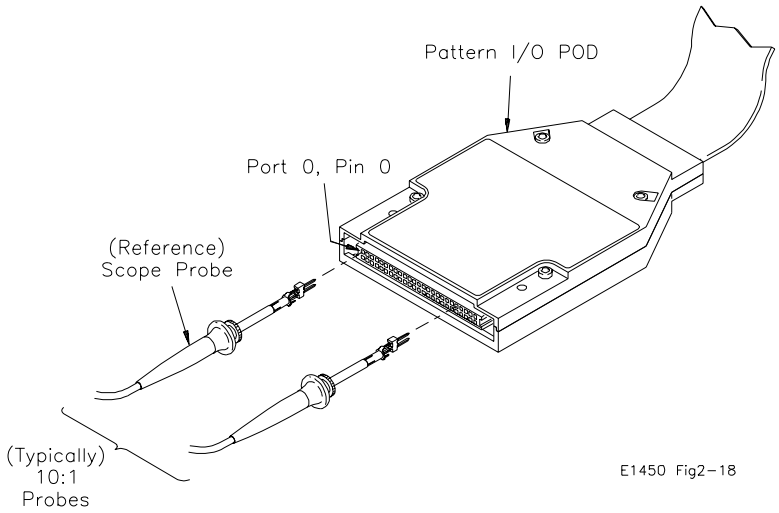

Figure 2-18. Measuring Skew Between Two Pins

Load Test Program

- Insert *Model D20 Service Programs Disk* in disk drive
- Load test program with LOAD "PERF_VER"
- Press RUN
- Select "Test P-2: System Skew Accuracy"

Example Program

This program causes all pins on ports 0 through 3 of the selected Pattern I/O module to change states simultaneously. This test allows you to measure skew on all pins of the selected Pattern I/O Module and on all Timing Module CONTROL output ports. Skew is measured relative to port 0, pin 0. The test procedure is:

1. Measure rising edge skew for port 0, pin 1 of selected Pattern I/O Module.
2. Record the skew on the Performance Test Record (Table 2-3).
3. Repeat steps 1 through 3 for remaining pins and CONTROL outputs.
4. Repeat steps 1 through 3 for falling edge skew measurements FOR THE PATTERN I/O PORTS ONLY.
5. Find maximum rising edge, falling edge, and CONTROL output skews. If maximums are < 6 nsec, the test passes.
6. Repeat steps 1 through 5 for the next selected Pattern I/O Module.

```
1   !Test P-2: System Skew Accuracy
2   !
10  CLEAR SCREEN
20  Addr=70917                                                    !Default Model D20 address = 70917
30  INPUT " Enter the Model D20 address (70917 is default) ",Addr !Assign Model D20 address
40  ASSIGN @Dft TO Addr
50  INPUT " Enter the Pattern I/O Module to be tested (1,2,...) ",Mod_no!Pattern I/O module to be tested
60  OUTPUT @Dft;"*RST"                                            !Set instrument to known state
70  OUTPUT @Dft;"SEQ:DEL:ALL"                                     !Delete all previous sequences
80  OUTPUT @Dft;"SEQ:DEF TEST_1,6"                                !Sequence "TEST_1" has 6 vectors
90  OUTPUT @Dft;"SEQ TEST_1"                                      !Select "TEST_1"
91  !----------------------------------------------------Set up Port 0 Pattern ----------------------------------------------------
100 OUTPUT @Dft;"GRO:DEL:ALL"                                     !Delete all previous groups
110 OUTPUT @Dft;"GRO:DEF OUT0,(@"&VAL$(Mod_no)&"(0))"             !Group "OUT0" uses port 0
120 OUTPUT @Dft;"GRO OUT0"                                        !Select OUT0"
130 OUTPUT @Dft;"GRO:MODE STIM"                                   !Set group mode to STIMulus
140 OUTPUT @Dft;"STIM:ENAB:SEQ:PART 0,1,1,1,1,1,1"                !Enables all vectors
150 OUTPUT @Dft;"STIM:PATT:SEQ:PART 0,0,255,0,255,0,255"          !Output HIGH on vectors 1,3,5 and
                                                                  LOW on vectors 0,2,4
```

(continued on next page)

```
160 OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                          !Use STIMulus clock 0
161 !----------------------------------------Set up Port 1 Pattern ----------------------------------------
170 OUTPUT @Dft;"GRO:DEF OUT1,(@"&VAL$(Mod_no)&"(1))"          !Group OUT1 uses port 1
180 OUTPUT @Dft;"GRO OUT1"                                     !Select "OUT1"
190 OUTPUT @Dft;"GRO:MODE STIM"                                !Set group mode to STIMulus
200 OUTPUT @Dft;"STIM:ENAB:SEQ:PART 0,1,1,1,1,1,1"             !Enable all vectors
210 OUTPUT @Dft;"STIM:PATT:SEQ:PART 0,0,255,0,255,0,255"       !Output HIGH on vectors 1,3,5 and
                                                               LOW on vectors 0,2,4
220 OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                          !Use STIMulus clock 0
221 !----------------------------------------Set up Port 2 Pattern ----------------------------------------
230 OUTPUT @Dft;"GRO:DEF OUT2,(@"&VAL$(Mod_no)&"(2))"          !Group "OUT2" uses port 2
240 OUTPUT @Dft;"GRO OUT2"                                     !Select "OUT2"
250 OUTPUT @Dft;"GRO:MODE STIM"                                !Set group mode to STIMulus
260 OUTPUT @Dft;"STIM:ENAB:SEQ:PART 0,1,1,1,1,1,1"             !Enable all vectors
270 OUTPUT @Dft;"STIM:PATT:SEQ:PART 0,0,255,0,255,0,255"       !Output HIGH on vectors 1,3,5 and
                                                               LOW on vectors 0,2,4
280 OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                          !Use STIMulus clock 0
281 !----------------------------------------Set up Port 3 Pattern ----------------------------------------
290 OUTPUT @Dft;"GRO:DEF OUT3,(@"&VAL$(Mod_no)&"(3))"          !Group "OUT3" uses port 3
300 OUTPUT @Dft;"GRO OUT3"                                     !Select "OUT3"
310 OUTPUT @Dft;"GRO:MODE STIM"                                !Set group mode to STIMulus
320 OUTPUT @Dft;"STIM:ENAB:SEQ:PART 0,1,1,1,1,1,1"             !Enable all vectors
330 OUTPUT @Dft;"STIM:PATT:SEQ:PART 0,0,255,0,255,0,255"       !Output HIGH on vectors 1,3,5 and
                                                               LOW on vectors 0,2,4
340 OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                          !Use STIMulus clock 0
341 !----------------------------------------Set up Timing Cycle ----------------------------------------
350 OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                             !Delete all previous timing cycles
360 OUTPUT @Dft;"TIM:CYCL:DEF TC_1,6"                          !Timing cycle "TC_1" has 6 subcycles
370 OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,6,TC_1"                    !Assign "TC_1" to all vectors
380 OUTPUT @Dft;"TIM:RES MIN"                                  !Each subcycle = 6.25 nsec
381 !----------------------------------------Set up CONTROL Outputs ----------------------------------------
390 OUTPUT @Dft;"TIM:CYCL TC_1"                                !Select timing cycle "TC_1"
400 OUTPUT @Dft;"TIM:CYCL:CONT0:WAV 1,5"                       !CONT0 HIGH @ cycle 1, LOW at  5
410 OUTPUT @Dft;"TIM:CYCL:CONT1:WAV 1,5"                       !CONT1 HIGH @ cycle 1, LOW at 5
420 OUTPUT @Dft;"TIM:CYCL:CONT2:WAV 1,5"                       !CONT2 HIGH @ cycle 1, LOW at 5
430 OUTPUT @Dft;"TIM:CYCL:CONT3:WAV 1,5"                       !CONT3 HIGH @ cycle 1, LOW at 5
440 OUTPUT @Dft;"TIM:CYCL:CONT4:WAV 1,5"                       !CONT4 HIGH @ cycle 1, LOW at 5
450 OUTPUT @Dft;"TIM:CYCL:CONT5:WAV 1,5"                       !CONT5 HIGH @ cycle 1, LOW at 5
460 OUTPUT @Dft;"TIM:CYCL:CONT6:WAV 1,5"                       !CONT6 HIGH @ cycle 1, LOW at 5
470 OUTPUT @Dft;"TIM:CYCL:CONT7:WAV 1,5"                       !CONT7 HIGH @ cycle 1, LOW at 5
```

(continued on next page)

```
480  OUTPUT @Dft;"TIM:CONT ON"                                  !Enable CONTROL outputs
481  !----------------------------------Set up LOOP operation ----------------------------------------------------
490  OUTPUT @Dft;"TIM:MARK:SEQ:PART 0,0,0,0,0,0,0"              !Disable marker outputs
500  OUTPUT @Dft;"DIAG:SEQ:LOOP:BOUN 0,5"                       !Loop from vector 0 through 5
510  OUTPUT @Dft;"DIAG:SEQ:LOOP ON"                             !Enable looping
520  OUTPUT @Dft;"RUN"                                          !RUN program
530  DISP " Record skews as desired. Then, press Continue "
540  PAUSE
550  CLEAR SCREEN
560  OUTPUT @Dft;"*RST"                                         !Reset instrument
570  END
```

Typical Results

Figures 2-19 through 2-21 illustrate typical waveforms for STIMulus pin rising and falling signals and for rising signal CONTROL port outputs. All signals should be within 6 nsec of the output on port 0, pin 0. Three example displays follow.

NOTE

Typically, 10:1 probes are used to input the signal to the oscilloscope. If you have difficulty obtaining the waveforms shown, check your oscilloscope settings to ensure a 10:1 probe setting, as required.

Rising Signal Skew - Pattern I/O Ports

Figure 2-19 shows a typical result for rising edge skew between pattern I/O port 0, pin 0 and port 2, pin 3. Since the waveform for port 0, pin 0 crosses the 1.6V threshold at -440 psec and the waveform for port 2, pin 3 crosses at +240 ps, skew for port 3, pin 2 = 240 psec -(-440 psec) = 680 psec = 0.68 nsec.

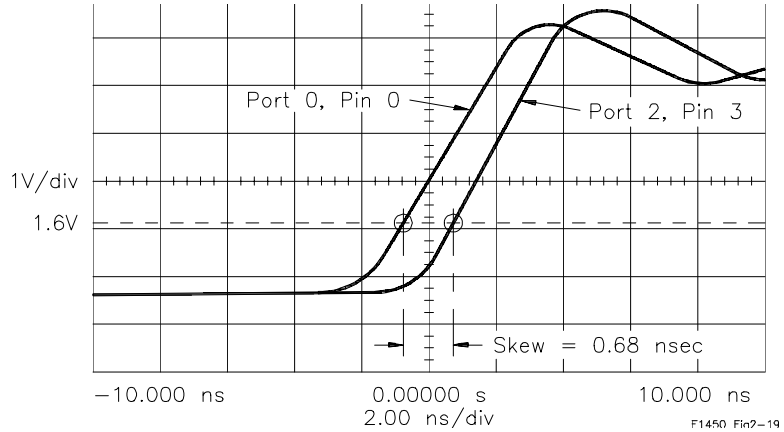

Figure 2-19. Rising Signal Skew - Pattern I/O Ports

Falling Signal Skew - Pattern I/O Ports

Figure 2-20 shows a typical result for falling edge skew between pattern I/O port 0, pin 0 and port 2, pin 3. Since the waveform for port 0, pin 0 crosses the 1.6V threshold at 40.76 nsec and the waveform for port 2, pin 3 crosses at 41.12 nsec, skew for port 3, pin 2 = 41.12 nsec - 40.76 nsec = 0.36 nsec.

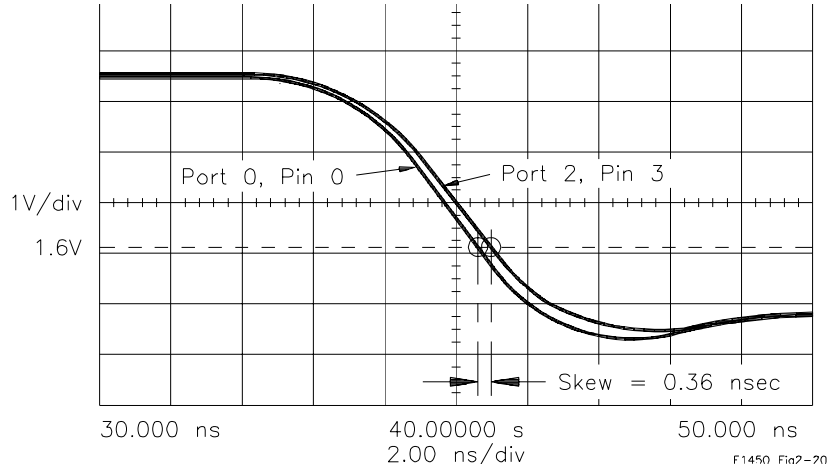

Figure 2-20. Falling Signal Skew - Pattern I/O Ports

Rising Signal Skew - CONTROL Ports

Figure 2-21 shows a typical result for rising edge skew between pattern I/O port 0, pin 0 and CONTROL port 0. Since the waveform for port 0, pin 0 crosses the 1.6V threshold at -440 psec and the waveform for CONTROL port 0 crosses at -680 psec, skew for CONTROL port 0 = -440 psec - (-680 psec) = 240 psec = 0.24 nsec. (For this program, there is no falling edge skew test for CONTROL ports.)

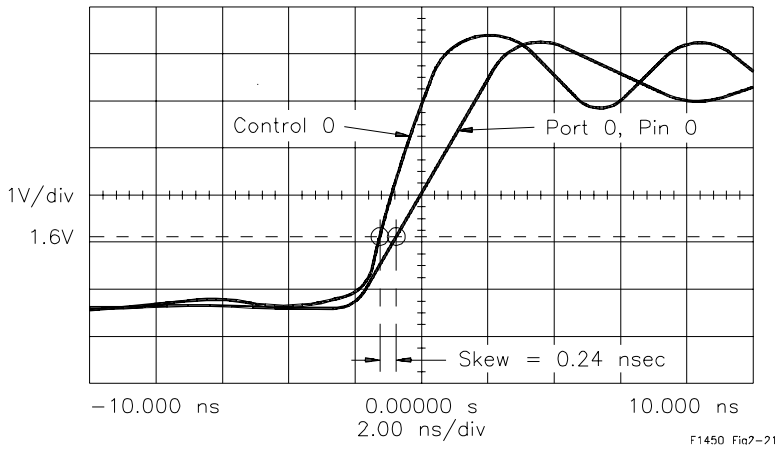

Figure 2-21. Rising Signal Skew - CONTROL Ports

Performance Test Record

Table 2-3, *Model D20 Performance Test Record*, can be used to record the results of the two Performance Verification test for the Model D20 (this record can be copied if desired). The record includes the upper and lower limits, the measurement uncertainty, and the Test Accuracy Ratio (TAR) (as applicable) for the test.

Measurement Uncertainty

For Test P-1: Subcycle Period Accuracy , "Measurement Uncertainty" is the accuracy of the Agilent 5334B Universal Counter used to measure the frequency. The Agilent 5334B accuracy = ±Resolution ±Time Base Error. From the Agilent 5334B specifications for a 1.6 MHz measurement, measurement uncertainty = ±1 Hz (resolution) ±2 Hz (Time Base Error) =±3 Hz.

For Test P-2: System Skew Accuracy, "Measurement Uncertainty" is the accuracy of the Agilent 54111D oscilloscope. From the Agilent 54111D specifications, time measurement accuracy for a single channel, repetitive measurement =±100 ps ± 0.03% of reading. Thus, for a 1 nsec skew reading, measurement uncertainty = ±100 ps ± .0003 x 1000 ps = ±100.3 ps.

Test Accuracy Ratio (TAR)

For Test P-1: Subcycle Period Accuracy, Test Accuracy Ratio (TAR) =Measurement Accuracy /Measurement Uncertainty, rounded to the nearest integer. Thus, TAR =±0.0001 MHz/3.0 Hz = ±100/3 = ±33:1 (rounded to the nearest integer).

Since Test P-2: System Skew Accuracy is defined as a single-ended test (no mimimum specified), TAR is not applicable (NA) as TARs are not defined for single-ended tests.

Table 2-3. Model D20 Performance Test Record (Page 1 of 3)

Test Facility:

Name _____

Address_____

City/State_____

Phone_____

Report No._____

Date_____

Customer_____

Tested by_____

Model_____

Serial No._____

Options_____

Firmware Rev._____

Ambient temperature_____^{o}C

Relative humidity_____%

Line frequency _____ Hz (nominal)

Test Equipment Used: Description	Model No.	Trace No.	Cal Due Date
1._____	_____	_____	_____
2. _____	_____	_____	_____
3. _____	_____	_____	_____
4. _____	_____	_____	_____
5. _____	_____	_____	_____
6. _____	_____	_____	_____
7. _____	_____	_____	_____
8. _____	_____	_____	_____
9. _____	_____	_____	_____
10. _____	_____	_____	_____
11. _____	_____	_____	_____

Table 2-3. Model D20 Performance Test Record (Page 2 of 3)

Model _____ Report No. _____ Date _____

Test No/Description	Minimum Value*	Measured Value	Maximum Value	Measurement Uncertainty	Test Acc Ratio (TAR)
P-1: Subcycle Period Accuracy					
	1.5999 MHz	_____	1.6001 MHz	±3.0 Hz	33:1
P-2: System Skew Accuracy (skew compared to Port 0, Pin 0)					
Rising Signals					
port 0, pin 1		_____	6 nsec	±100.3 psec	NA
port 0, pin 2		_____			
port 0, pin 3		_____			
port 0, pin 4		_____			
port 0, pin 5		_____			
port 0, pin 6		_____			
port 0, pin 7		_____			
port 1, pin 0		_____			
port 1, pin 1		_____			
port 1, pin 2		_____			
port 1, pin 3		_____			
port 1, pin 4		_____			
port 1, pin 5		_____			
port 1, pin 6		_____			
port 1, pin 7		_____			
port 2, pin 0		_____			
port 2, pin 1		_____			
port 2, pin 2		_____			
port 2, pin 3		_____			
port 2, pin 4		_____			
port 2, pin 5		_____			
port 2, pin 6		_____			
port 2, pin 7		_____			
port 3, pin 0		_____			
port 3, pin 1		_____			
port 3, pin 2		_____			
port 3, pin 3		_____			
port 3, pin 4		_____			
port 3, pin 5		_____			
port 3, pin 6		_____			
port 3, pin 7		_____			

* Test P-2 is single-sided specification - Minimum value does not apply

Table 2-3. Model D20 Performance Test Record (Page 3 of 3)

Model _____ Report No. _____ Date _____

Test No/Description	Minimum Value*	Measured Value (nsec)	Maximum Value	Measurement Uncertainty	Test Acc Ratio (TAR)
P-2: System Skew Accuracy (skew compared to Port 0, Pin 0) (cont'd)					
CONTROL 0		_____	6 nsec	±100.3 psec	NA
CONTROL 1		_____	↓	↓	↓
CONTROL 2		_____			
CONTROL 3		_____			
CONTROL 4		_____			
CONTROL 5		_____			
CONTROL 6		_____			
CONTROL 7		_____			
Falling Signals					
		_____			
port 0, pin 1		_____			
port 0, pin 2		_____			
port 0, pin 3		_____			
port 0, pin 4		_____			
port 0, pin 5		_____			
port 0, pin 6		_____			
port 0, pin 7		_____			
port 1, pin 0		_____			
port 1, pin 1		_____			
port 1, pin 2		_____			
port 1, pin 3		_____			
port 1, pin 4		_____			
port 1, pin 5		_____			
port 1, pin 6		_____			
port 1, pin 7		_____			
port 2, pin 0		_____			
port 2, pin 1		_____			
port 2, pin 2		_____			
port 2, pin 3		_____			
port 2, pin 4		_____			
port 2, pin 5		_____			
port 2, pin 6		_____			
port 2, pin 7		_____			
port 3, pin 0		_____			
port 3, pin 1		_____			
port 3, pin 2		_____			
port 3, pin 3		_____			
port 3, pin 4		_____			
port 3, pin 5		_____			
port 3, pin 6		_____			
port 3, pin 7		_____			

* Test P-2 is single-sided specification - Minimum value does not apply

3
Replaceable Parts

Introduction

This chapter contains information to order replaceable parts for Agilent 75000 Model D20 components shown in Table 3-1.

Table 3-1. Applicable Components/Descriptions

Component	Description	Serial # Prefix
Agilent E1450A	160 MHz Timing Module	ALL
Agilent E1451A	20 MHz Pattern I/O Module	ALL
Agilent E1452A	20 MHz Term Pattern I/O Module	ALL
Agilent E1453A	Timing Pod	ALL
Agilent E1454A	Pattern I/O Pod	ALL
Agilent E1455A	Timing Pod (Mac Panel)	ALL
Agilent E1456A	Pattern I/O Pod (Mac Panel)	ALL
Agilent 91474A	D20 Block ICA (Mac Panel)	N/A
	LIght Board	N/A
	E1450A/51A/52A Interface Cables	N/A

Replaceable Parts Lists

Table 3-4 lists replaceable parts for Agilent 75000 Model D20 instruments, Table 3-2 shows reference designators for parts in Table 3-4, and Table 3-3 shows the manufacturer code list for these parts.

Exchange Assemblies

Table 3-4 lists assemblies that may be replaced on an exchange basis (EXCHANGE). Exchange assemblies are available only on a trade-in basis. Defective assemblies must be returned for credit. Order assemblies for spare parts stock by the new assembly part number.

Ordering Information

To order a part listed in Table 3-4, specify the Agilent part number and the quantity required. Send the order to your nearest Agilent Technologies Sales and Service Office.

Field Installation Kits

Two field installation kits are available for the Model D20. To provide a downloadable Model D20 SCPI driver for the Agilent E1405B Command Module, order kit E1450-80001. For compliance with German EMI Standards, order the Backplane Connector Shield Kit (E1450-80920). Order kits from your nearest Agilent Technologies Sales and Support Office.

Model D20 Replaceable Parts Lists

Table 3-4 lists replaceable parts for Agilent 75000 Model D20 instruments with serial number prefixes shown in Table 3-1. See *Model D20 Component Locators* (Figures 3-1 through 3-17) for locations of parts in Table 3-4. Table 3-2 shows reference designators for parts in Table 3-4, while Table 3-3 shows the manufacturer code list for these parts.

NOTE

If a module defect can be traced to a fuse, replace the fuse and test the module before returning the module to Agilent Technologies. If the defect cannot be traced to a fuse, troubleshoot (as desired) to the component level, but do not attempt repairs. Return the module or pod (with a description of the defect, if known) to Agilent Technologies for replacement or exchange.

Table 3-2. Agilent 75000 Model D20 Reference Designators

Agilent 75000 MODEL D20 REFERENCE DESIGNATORS		
A ..... assembly	J .....electrical connector (jack)	S ..... switch (rotary)
CBL ..... cable	MP ..... misc. mech part	SCR ..... screw
CVR .....cover	NUT .....nut	SHD ..... shield
F ..... fuse	P ..... electrical conn (plug)	SP ..... switch (push-button)
HD or HW .....misc hardware	PNL ..... panel	

Table 3-3. Agilent 75000 Model D20 Code List of Manufacturers

Mfr Code	Manufacturer Name	Address
00000	Any Satisfactory Supplier	
06776	Robinson Nugent, Inc	New Albany, IN 47150
09441	Applied Engineering Products Co	Hamden, CT 06514
18873	Dupont E. I. de Nemours & Co	Wilmington, DE 19801
24840	Agilent Technologies - Corporate	Palo Alto, CA 94304
30817	Instrument Specialties, Inc	Del Water Gap, PA 07424
74163	Phelps Dodge Corp	New York, NY 10022
74970	E. F. Johnson Co	Waseca, MN 56093
75915	Littlefuse, Inc	Des Plaines, IL 60016
76381	3M Co	St. Paul, MN 55144
81073	Grayhill, Inc	La Grange, IL 60525
83486	Elco Industries, Inc	Rockford, IL 61125
93907	Camcar Screw & Mfg Co	Rockford, IL 61101
98921	ITT Sealectro Corp	Trumbull, CT 06611

Table 3-4. Agilent 75000 Model D20 Replaceable Parts

Reference* Designator	Agilent Part Number	Qty	Description	Mfr** Code	Mfr Part Number
Agilent E1450A TIMING MODULE PARTS					
			E1450A NEW/EXCHANGE ASSEMBLIES		
	E1450-66201	1	E1450A TIMING MODULE (NEW)	28480	E1450-66201
	E1450-69201	1	E1450A TIMING MODULE (EXCHANGE)	28480	E1450-69201
			E1450A CHASSIS PARTS (FIGS 3-1 - 3-3)		
	1250-2076	1	TERMINATION - 50 OHM CONNECTOR	09441	2036-1511-151
CBL1	E1450-61601	1	20-PIN JUMPER CABLE	28480	E1450-61601
CBL2	E1450-61602	1	40-PIN CABLE	28480	E1450-61602
HDL1	E1400-84105	1	EXT HNDL KIT - BTM	28480	E1400-84105
HDL2	E1400-84106	1	EXT HNDL KIT - TOP	28480	E1400-84106
MNL1	E1450-90001	1	MANUAL - HARDWARE	28480	E1450-90001
PNL1	E1450-00201	1	FRONT PANEL	28480	E1450-00201
SHD1	E1450-00601	1	BACK SHIELD	28480	E1450-00601
SHD2	E1450-00602	1	TOP SHIELD	28480	E1450-00602
			E1450A A1 PCA (SLOT 0) PARTS (FIG 3-4)		
A1	E1450-66501	1	A1 PCA (TIMING MODULE SLOT 0)	28480	E1450-66501
F1501	2110-0713	3	FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F1502	2110-0713		FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F1503	2110-0713		FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
J901	1250-2266	3	CONN-RF SMB M PC-W-STDFS 50-OHM	74970	131-3701-501
J902	1250-2266		CONN-RF SMB M PC-W-STDFS 50-OHM	74970	131-3701-501
J903	1250-2266		CONN-RF SMB M PC-W-STDFS 50-OHM	74970	131-3701-501
J1601	1252-4175	3	CONN-RECT MICRORBN 20-CKT 20-CONT	76381	10220-52B2VE
J1602	1252-4175		CONN-RECT MICRORBN 20-CKT 20-CONT	76381	10220-52B2VE
J1603	1252-4175		CONN-RECT MICRORBN 20-CKT 20-CONT	76381	10220-52B2VE
J1604	1252-4176	1	CONN-RECT MICRORBN 50-CKT 50-CONT	76381	10220-52B2VE
J1605	1251-8828	1	CONN-POST TYPE .100-PIN-SPCG-40-CONT	76381	2540-6002UB
P1601	1252-1596	1	CONN-POST TYPE 2.54-PIN-SPCG-96-CONT	06776	DIN-96CPC-SRI-TR
P1602	1251-7892	1	CONN-POST TYPE 2.54-PIN-SPCG-64-CONT	18873	75882-364
			E1450A A2 PCA (SLOT 1) PARTS (FIG 3-5)		
A2	E1450-66502	1	A2 PCA (TIMING MODULE SLOT 1)	28480	E1450-66502
F1401	2110-0713	3	FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F1402	2110-0713		FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F1403	2110-0713		FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
J1101	1250-2266	2	CONN-RF SMB M PC-W-STDFS 50-OHM	74970	131-3701-501
J1102	1250-2266		CONN-RF SMB M PC-W-STDFS 50-OHM	74970	131-3701-501
J1401	1251-8828	1	CONN-POST TYPE .100-PIN-SPCG-40-CONT	76381	2540-6002UB
P1401	1252-1596	1	CONN-POST TYPE 2.54-PIN-SPCG-96-CONT	06776	DIN-96CPC-SRI-TR
P1402	1251-7892	1	CONN-POST TYPE 2.54-PIN-SPCG-64-CONT	18873	75882-364

* See Table 3-2 for Reference Designator definitions
** See Table 3-3 for Code List of Manufacturers

Table 3-4. Agilent 75000 Model D20 Replaceable Parts (cont'd)

Reference* Designator	Agilent Part Number	Qty	Description	Mfr** Code	Mfr Part Number
			E1450A HARDWARE PARTS (FIGs 3-1 - 3-3)		
HDW1	0380-3059	2	STANDOFF - HEX M3.0 X 0.5-THD SST-303 PSVT	28480	0380-3059
HDW2	0380-3059		STANDOFF - HEX M3.0 X 0.5-THD SST-303 PSVT	28480	0380-3059
HWD1	2190-0124	5	WASHER-LK INTL T NO. 10 .195-IN-ID	98291	3002-26
HWD2	2190-0124		WASHER-LK INTL T NO. 10 .195-IN-ID	98291	3002-26
HWD3	2190-0124		WASHER-LK INTL T NO. 10 .195-IN-ID	98291	3002-26
HWD4	2190-0124		WASHER-LK INTL T NO. 10 .195-IN-ID	98291	3002-26
HWD5	2190-0124		WASHER-LK INTL T NO. 10 .195-IN-ID	98291	3002-26
MP1	8160-0686	1	CLIP-RFI STRIP-FINGERS BE-CU SN-PL	30817	00786-185
MP2	E1450-01202	8	EMI STRIP	28480	E1450-01202
MP3	E1450-01202		EMI STRIP	28480	E1450-01202
MP4	E1450-01202		EMI STRIP	28480	E1450-01202
MP5	E1450-01202		EMI STRIP	28480	E1450-01202
MP6	E1450-01202		EMI STRIP	28480	E1450-01202
MP7	E1450-01202		EMI STRIP	28480	E1450-01202
MP8	E1450-01202		EMI STRIP	28480	E1450-01202
MP9	E1450-01202		EMI STRIP	28480	E1450-01202
MP10	E1450-01203	2	RFI CLIPS	28480	E1450-01203
MP11	E1450-01203		RFI CLIPS	28480	E1450-01203
MP13	E1450-01204	2	RFI BLOCKS	28480	E1450-01204
MP14	E1450-01204		RFI BLOCKS	28480	E1450-01204
MP15	1250-2076	1	FEMALE SMB; 51 OHM + -5%, 1/2 WATT RESISTANCE	28480	1250-2076
NUT1	2950-0078	5	NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	74163	500220
NUT2	2950-0078		NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	74163	500220
NUT3	2950-0078		NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	74163	500220
NUT4	2950-0078		NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	74163	500220
NUT5	2950-0078		NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	74163	500220
SCR1	0515-1227	15	SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR2	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR3	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR4	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR5	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR6	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR7	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR8	0515-0430	2	SCR-PHM 3 X 6 MM TX SC	28480	0515-0430
SCR9	0515-0430		SCR-PHM 3 X 6 MM TX SC	28480	0515-0430
SCR10	0515-1375	16	SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR11	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR12	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR13	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR14	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR15	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR16	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR17	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR18	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR19	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR20	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR21	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR22	0515-1968	4	SCR-PHM 2.5 X 11 MM TX	28480	0515-1968
SCR23	0515-1968		SCR-PHM 2.5 X 11 MM TX	28480	0515-1968
SCR24	0515-1968		SCR-PHM 2.5 X 11 MM TX	28480	0515-1968
SCR25	0515-1968		SCR-PHM 2.5 X 11 MM TX	28480	0515-1968
SCR26	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR27	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR28	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR29	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227

* See Table 3-2 for Reference Designator definitions
** See Table 3-3 for Code List of Manufacturers

Table 3-4. Agilent 75000 Model D20 Replaceable Parts (cont'd)

Reference* Designator	Agilent Part Number	Qty	Description	Mfr** Code	Mfr Part Number
			E1450A HARDWARE PARTS (CONT'D)		
SCR30	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR31	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR32	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR33	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR34	0515-1375		SCR-FHM 2.5 X 6 MM TX	28480	0515-1375
SCR35	0515-1375		SCR-FHM 2.5 X 6 MM TX	28480	0515-1375
SCR36	0515-0368	2	SCR-PHM 2.5 X 12 MM TX	28480	0515-0368
SCR37	0515-0368		SCR-PHM 2.5 X 12 MM TX	28480	0515-0368
SCR38	0515-1375		SCR-FHM 2.5 X 6 MM TX	28480	0515-1375
SCR39	0515-1375		SCR-FHM 2.5 X 6 MM TX	28480	0515-1375

Agilent E1451A PATTERN I/O MODULE PARTS

			E1451A PATTERN I/O NEW/EXCHANGE ASSYS		
	E1451-66201	1	E1451A PATTERN I/O MODULE (NEW)	28480	E1451-66201
	E1451-69201	1	E1451A PATTERN I/O MODULE (EXCHANGE)	28480	E1451-69201
			E1451A CHASSIS PARTS (FIG 3-6)		
HDL1	E1400-84105	1	EXT HNDL KIT - BTM	28480	E1400-84105
HDL2	E1400-84106	1	EXT HNDL KIT - TOP	28480	E1400-84106
MNL1	E1451-90001	1	MANUAL - HARDWARE	28480	34510-67900
PNL1	E1451-00201	1	FRONT PANEL	28480	E1451-00201
SHD1	E1451-00601	1	TOP SHIELD	28480	E1451-00601
SHD2	E1451-00602	1	BOTTOM SHIELD	28480	E1451-00602
			E1451A A1 PCA PARTS (FIG 3-7)		
A1	E1451-66503	1	A1 PCA (PATTERN I/O MODULE)	28480	E1451-66503
F101	2110-0713	3	FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F102	2110-0713		FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F103	2110-0713		FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F104	2110-0665	1	FUSE-SUBMINIATURE 1A 125V NTD AX UL CSA	75915	R251001T1
J1401	1252-4176	2	CONN-RECT MICRORBN 50-CKT 50-CONT	76381	10250-52B2VE
J1501	1252-4176		CONN-RECT MICRORBN 50-CKT 50-CONT	76381	10250-52B2VE
P101	1252-1596	1	CONN-POST TYPE 2.54-PIN-SPCG 96-CONT	06776	DIN-96CPC-SRI-TR
P102	1251-7892	1	CONN-POST TYPE 2.54-PIN-SPCG 64-CONT	18873	75882-364
			E1451A HARDWARE PARTS (FIG 3-6)		
MP1	8160-0686	1	CLIP-RFI STRIP-FINGERS BE-CU SN-PL	30817	00786-185
MP2	E1450-01202	4	EMI STRIPS	28480	E1450-01202
MP3	E1450-01202		EMI STRIPS	28480	E1450-01202
MP4	E1450-01202		EMI STRIPS	28480	E1450-01202
MP5	E1450-01202		EMI STRIPS	28480	E1450-01202

* See Table 3-2 for Reference Designator definitions
** See Table 3-3 for Code List of Manufacturers

Table 3-4. Agilent 75000 Model D20 Replaceable Parts (cont'd)

Reference* Designator	Agilent Part Number	Qty	Description	Mfr** Code	Mfr Part Number
			E1451A HARDWARE PARTS (CONT'D)		
SCR1	0515-1135	7	SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR2	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR3	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR4	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR5	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR6	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR7	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR8	0515-1227	3	SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR9	0515-1968	2	SCR-PHM 2.5 X 11 MM TX	28480	0515-1968
SCR10	0515-1968		SCR-PHM 2.5 X 11 MM TX	28480	0515-1968
SCR11	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR12	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR15	0515-1375	6	SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR16	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR17	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR18	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR19	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR20	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR21	0515-0368	2	SCR-PHM 2.5 X 12 MM TX SC	28480	0515-0368
SCR22	0515-0368		SCR-PHM 2.5 X 12 MM TX SC	28480	0515-0368

Agilent E1452A TERMINATING PATTERN I/O MODULE PARTS

			E1452A TERM PATT I/O MOD NEW/EXCH ASSYS		
	E1452-66201	1	E1452A MODULE (NEW)	28480	E1452-66201
	E1452-69201	1	E1452A MODULE (EXCHANGE)	28480	E1452-69201
			E1452A HARDWARE PARTS (FIG 3-8)		
HDL1	E1400-84105	1	EXT HNDL KIT - BTM	28480	E1400-84105
HDL2	E1400-84106	1	EXT HNDL KIT - TOP	28480	E1400-84106
MNL1	E1451-90001	1	MANUAL - E1451/52 PATTERN I/O HSW	28480	E1451-90001
PNL1	E1452-00201	1	FRONT PANEL	28480	E1452-00201
SHD1	E1451-00601	1	TOP SHIELD	28480	E1451-00601
SHD2	E1451-00602	1	BOTTOM SHIELD	28480	E1451-00602
			E1452A A1 PCA PARTS (FIG 3-9)		
A1	E1452-66503	1	A1 PCA (TERMINATING PATTERN I/O MODULE)	28480	E1452-66503
F101	2110-0713	3	FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F102	2110-0713		FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F103	2110-0713		FUSE-SUBMINIATURE 10A 125V NTD AX UL CSA	75915	R251010T1
F104	2110-0665	1	FUSE-SUBMINIATURE 1A 125V NTD AX UL CSA	75915	R251001T1
J1401	1252-4176	2	CONN-RECT MICRORBN 50-CKT 50-CONT	76381	10250-52B2VE
J1501	1252-4176		CONN-RECT MICRORBN 50-CKT 50-CONT	76381	10250-52B2VE
P101	1252-1596	1	CONN-POST TYPE 2.54-PIN-SPCG 96-CONT	06776	DIN-96CPC-SRI-TR
P102	1251-7892	1	CONN-POST TYPE 2.54-PIN-SPCG 64-CONT	18873	75882-364

* See Table 3-2 for Reference Designator definitions
** See Table 3-3 for Code List of Manufacturers

Table 3-4. Agilent 75000 Model D20 Replaceable Parts (cont'd)

Reference* Designator	Agilent Part Number	Qty	Description	Mfr** Code	Mfr Part Number
			E1452A HARDWARE PARTS (FIG 3-8)		
MP1	8160-0686	1	CLIP-RFI STRIP-FINGERS BE-CU SN-PL	30817	00786-185
MP2	E1450-01202	4	EMI STRIPS	28480	E1450-01202
MP3	E1450-01202		EMI STRIPS	28480	E1450-01202
MP4	E1450-01202		EMI STRIPS	28480	E1450-01202
MP5	E1450-01202		EMI STRIPS	28480	E1450-01202
SCR1	0515-1135	7	SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR2	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR3	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR4	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR5	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR6	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR7	0515-1135		SCR-FHM 3 X 25 MM TX	28480	0515-1135
SCR8	0515-1227	3	SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR9	0515-1968	2	SCR-PHM 2.5 X 11 MM TX	28480	0515-1968
SCR10	0515-1968		SCR-PHM 2.5 X 11 MM TX	28480	0515-1968
SCR15	0515-1375	6	SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR16	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR17	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR18	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR19	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR20	0515-1375		SCR-FHM 2.5 X 6 MM TX	83486	343-300-02506
SCR21	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR22	0515-1227		SCR-FHM 3 X 6 MM TX	28480	0515-1227
SCR23	0515-0368	2	SCR-PHM 2.5 X 12 MM TX SC	28480	0515-0368
SCR24	0515-0368		SCR-PHM 2.5 X 12 MM TX SC	28480	0515-0368

Agilent E1453A TIMING POD PARTS

			E1453A HARDWARE PARTS (FIG 3-10)		
CBL1***	E1453-61601	1	50-PIN TIMING POD CABLE	28480	E1453-61601
CVR1	E1453-44101	1	COVER-TOP	28480	E1453-44101
CVR2	E1453-44102	1	COVER-BOTTOM	28480	E1453-44102
MNL1	E1453-01201	2	CABLE GROUND	28480	E1453-01201
MP1	E1453-01201		CABLE GROUND	28480	E1453-01201
MP1A	34510-67900	1	MNL, DISCS FOR 34509B/C	28480	34510-67900
PKG1	0624-0600	2	SCREW-TPG 4-20 .375-IN-LG -HD-TORX T10	28480	0624-0600
SCR1	0624-0600		SCREW-TPG 4-20 .375-IN-LG -HD-TORX T10	28480	0624-0600
SCR2	0624-0697	4	SCREW-TPG 4-20 .5-IN-LG PAN-HD-TORX T10	93907	225-08904-890
SCR3	0624-0697		SCREW-TPG 4-20 .5-IN-LG PAN-HD-TORX T10	93907	225-08904-890
SCR4	0624-0697		SCREW-TPG 4-20 .5-IN-LG PAN-HD-TORX T10	93907	225-08904-890
SCR5	0624-0697		SCREW-TPG 4-20 .5-IN-LG PAN-HD-TORX T10	93907	225-08904-890
SCR6					
			E1453A A1 PCA (TIMING POD) PARTS (FIG 3-11)		
A1	E1453-66501	1	A1 PCA (TIMING POD)	28480	E1453-66501
J1	1252-4408	1	CONN-POST TYPE 2.54-PIN-SPCG 50-CONT	76381	9A50-0500VE

* See Table 3-2 for Reference Designator definitions
** See Table 3-3 for Code List of Manufacturers
*** Rerun Performance Verification Tests after replacing

Table 3-4. Agilent 75000 Model D20 Replaceable Parts (cont'd)

Reference* Designator	Agilent Part Number	Qty	Description	Mfr** Code	Mfr Part Number
Agilent E1454A PATTERN I/O POD PARTS					
			E1454A HARDWARE PARTS (FIG 3-12)		
CBL1***	E1453-61601	1	50-PIN POD CABLE	28480	E1453-61601
CVR1	E1453-44101	1	COVER-TOP	28480	E1453-44101
CVR2	E1453-44102	1	COVER-BOTTOM	28480	E1453-44102
MP1	E1453-01201	2	CABLE GROUND	28480	E1453-01201
MP1A	E1453-01201		CABLE GROUND	28480	E1453-01201
PKG1	34510-67900	1	MNL, DISCS FOR 34509B/C	8480	34510-67900
SCR1	0624-0600	2	SCREW-TPG 4-20 .375-IN-LG -HD-TORX T10	28480	0624-0600
SCR2	0624-0600		SCREW-TPG 4-20 .375-IN-LG -HD-TORX T10	28480	0624-0600
SCR3	0624-0697	4	SCREW-TPG 4-20 .5-IN-LG PAN-HD-TORX T10	93907	225-08904-890
SCR4	0624-0697		SCREW-TPG 4-20 .5-IN-LG PAN-HD-TORX T10	93907	225-08904-890
SCR5	0624-0697		SCREW-TPG 4-20 .5-IN-LG PAN-HD-TORX T10	93907	225-08904-890
SCR6	0624-0697		SCREW-TPG 4-20 .5-IN-LG PAN-HD-TORX T10	93907	225-08904-890
			E1454A A1 PCA (PATT I/O POD) PARTS (FIG 3-13)		
A1	E1454-66501	1	A1 PCA (PATTERN I/O POD)	28480	E1454-66501
J2	1252-4408	1	CONN-POST TYPE 2.54-PIN-SPCG 50-CONT	76381	9A50-0500VE
Agilent E1455A TIMING POD (MAC PANEL) PARTS					
			E1455A CHASSIS PARTS (FIG 3-14)		
CBL1***	E1453-61603	1	50-PIN POD CABLE	28480	E1453-61601
CVR1	E1455-00601	1	COVER-TOP	28480	E1455-00601
CVR2	E1455-00602	1	COVER-BOTTOM	28480	E1455-00602
MP1	E1453-01202	2	CABLE GROUND	28480	E1453-01202
MP1A	E1453-01202		CABLE GROUND	28480	E1453-01202
MP3	E1455-00603	1	INSULATOR	28480	E1455-00603
MP4	E1455-21201	1	CABLE CLAMP	28480	E1455-21201
SCR1	0515-2032	7	SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR2	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR3	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR4	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR5	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR6	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR7	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
			E1455A A1 PCA PARTS (FIG 3-14)		
A1	E1455-66501	1	A1 PCA (TIMING POD - MAC PANEL)	28480	E1455-66501
J1	5061-1691	1	HDI CONNECTOR WITH LEADS CUT	28480	5061-1691
J2	1252-4303	1	CONN-POST TYPE .050-PIN-SPCG 50-CONT	76381	81050-560203

* See Table 3-2 for Reference Designator definitions
** See Table 3-3 for Code List of Manufacturers
*** Rerun Performance Verification Tests after replacing

Table 3-4. Agilent 75000 Model D20 Replaceable Parts (cont'd)

Reference* Designator	Agilent Part Number	Qty	Description	Mfr** Code	Mfr Part Number
Agilent E1456A PATTERN I/O POD (MAC PANEL) PARTS					
			E1456A CHASSIS PARTS (FIG 3-15)		
CBL1***	E1454-61602	1	50-PIN CABLE	28480	E1454-61602
CVR1	E1456-00601	1	COVER-TOP	28480	E1455-00601
CVR2	E1455-00602	1	COVER-BOTTOM	28480	E1455-00602
MP1	E1453-01202	2	CABLE GROUND	28480	E1453-01202
MP1A	E1453-01202		CABLE GROUND	28480	E1453-01202
MP3	E1455-00603	1	INSULATOR	28480	E1455-00603
MP4	E1455-21201	1	CABLE CLAMP	28480	E1455-21201
SCR1	0515-2032	7	SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR2	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR3	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR4	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR5	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR6	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
SCR7	0515-2032		SCREW-MACH M3 X 0.5 8MM-LG 90-DEG-FLH-HD	28480	0515-2032
			E1456A A1 PCA PARTS (FIG 3-15)		
A1	E1456-66501	1	A1 PCA (I/O POD - MAC PANEL)	28480	E1456-66501
J1	1252-4303	1	CONN-POST TYPE .050-PIN-SPCG 50-CONT	76381	81050-560203
J2	5061-1691	1	HDI CONNECTOR WITH LEADS CUT	28480	5061-1691
Agilent 91474A D20 BLOCK ICA PARTS					
	91474-60001	1	MODEL D20 CONNECTOR BLOCK ASSEMBLY	28480	91474-60001
LIGHT BOARD PARTS					
			LIGHT BOARD A1 PCA (FIG 3-16)		
A1	E1493-66502	1	A1 PCA (LIGHT BOARD)	28480	E1493-66502
J101	1251-8262	3	CONN-POST TYPE .100-PIN-SPCG 50-CONT	76381	2550-6002UB
J102	1251-8262		CONN-POST TYPE .100-PIN-SPCG 50-CONT	76381	2550-6002UB
J103	1251-8262		CONN-POST TYPE .100-PIN-SPCG 50-CONT	76381	2550-6002UB
SP101	3101-3066	3	SWITCH-DIP RKR SPST 0.1A 5VDC	81073	76YY22968S
SP102	3101-3066		SWITCH-DIP RKR SPST 0.1A 5VDC	81073	76YY22968S
SP103	3101-3066		SWITCH-DIP RKR SPST 0.1A 5VDC	81073	76YY22968S
Agilent E1450A/51A/52A INTERFACE CABLES					
			E1450A/51A/52A INTERFACE CABLES (FIG 3-17)		
	E1453-61602	1	INTERFACE CABLE - TIMING MOD TO DUT	28480	E1453-61602
	E1454-61601	2****	INTERFACE CABLE - PATTERN I/O MOD TO DUT	28480	E1454-61601

* See Table 3-2 for Reference Designator definitions
** See Table 3-3 for Code List of Manufacturers
*** Rerun Performance Verification Tests after replacing
**** Two cables per each Agilent E1451A and Agilent E1452A module

Model D20 Component Locators

Figures 3-1 through 3-17 show locations of selected replaceable parts for Agilent 75000 Model D20 components.

E1450A HARDWARE PARTS LEGEND

Letter	Description	Part No.	Qty.	Reference Designation
Ⓐ	Screw Assembly	0515-1375	2	SCR10 - SCR11
Ⓑ	Screw	0515-1375	14	SCR12 - SCR21, SCR34 - SCR35, SCR38 - SCR39
Ⓒ	Screw	0515-0430	2	SCR8 - SCR9
Ⓔ	Screw	0515-1227	15	SCR1 - SCR7, SCR26 - SCR29, SCR30 - SCR33
Ⓕ	Washer	2190-0124	5	HWD1 - HWD5
Ⓖ	Nut	2950-0078	5	NUT1 - NUT5

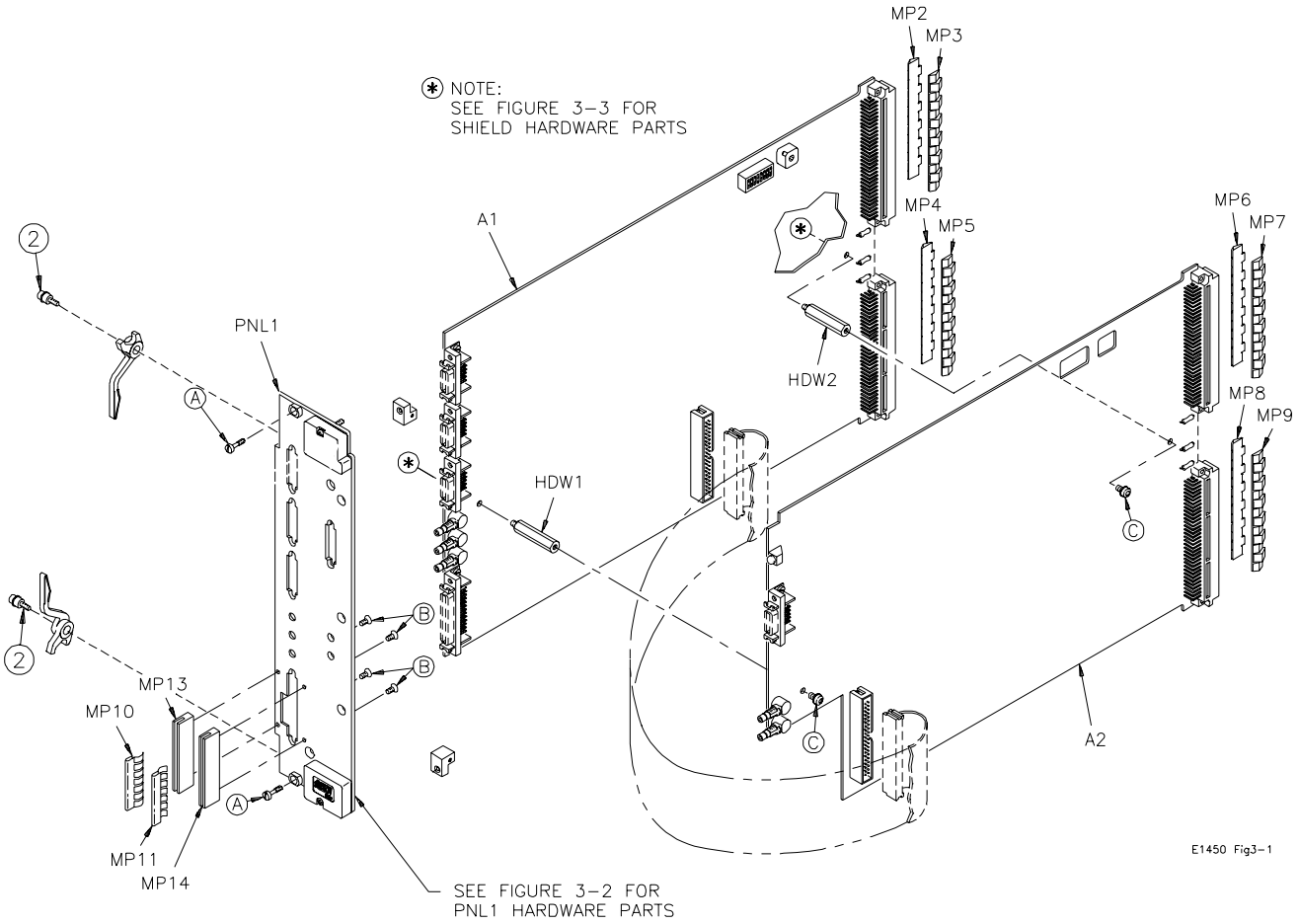

Figure 3-1. E1450A Timing Module - Hardware Parts

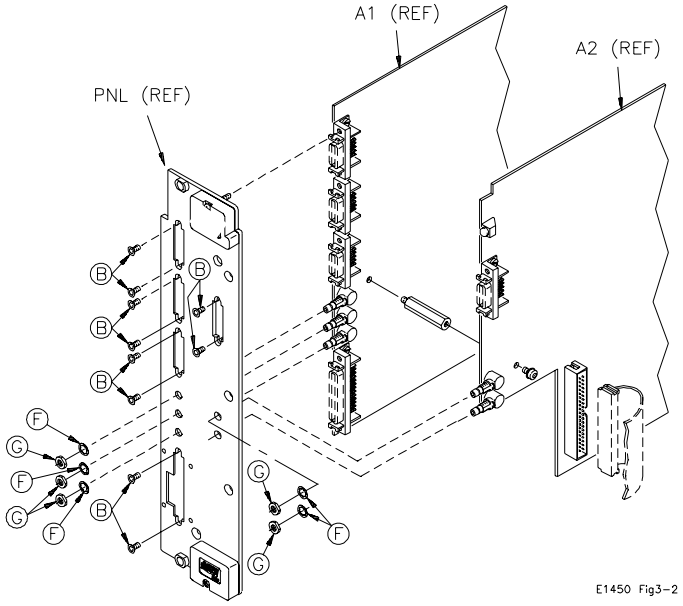

Figure 3-2. E1450A Timing Module - Front Panel

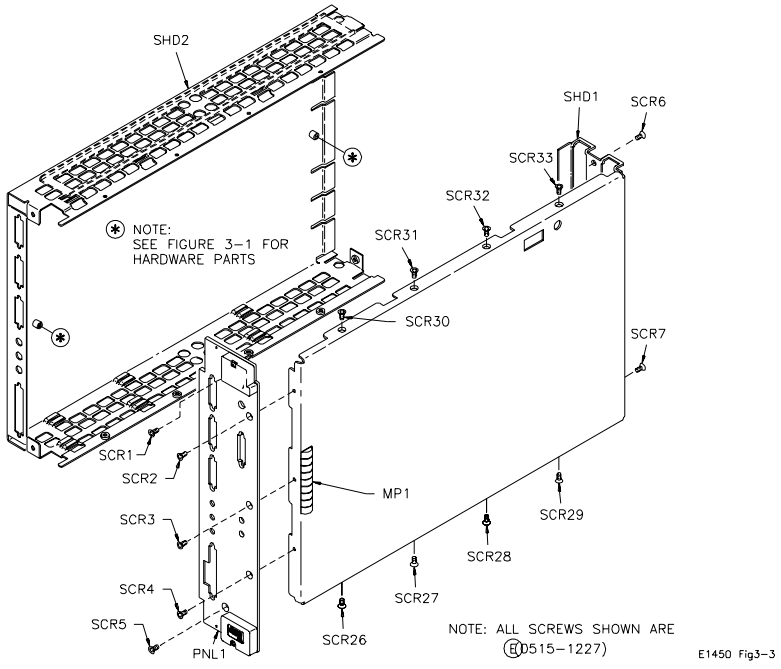

Figure 3-3. E1450A Timing Module - Shield Parts

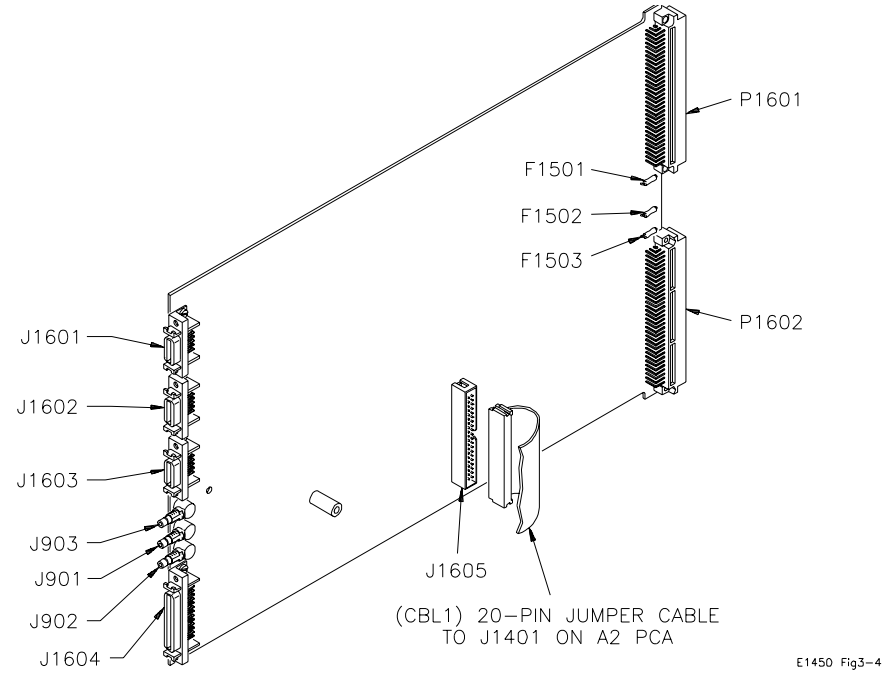

Figure 3-4. E1450A Timing Module - A1 PCA (Slot 0)

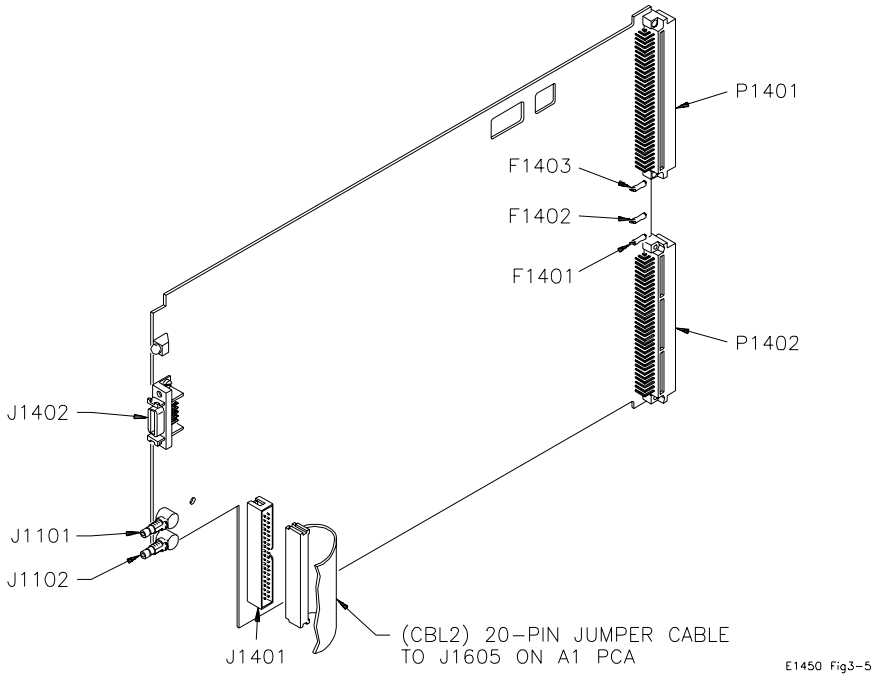

Figure 3-5. E1450A Timing Module - A2 PCA (Slot 1)

E1451A HARDWARE PARTS LEGEND

Letter	Description	Part No.	Qty.	Reference Designation
Ⓐ	Screw	0515-1135	7	SCR1 - SCR7
Ⓑ	Screw	0515-1227	3	SCR8, SCR11, SCR12
Ⓒ	Screw Assembly	E1400-00610	2	SCR15 - SCR16
Ⓓ	Screw	0515-1375	4	SCR12 - SCR20

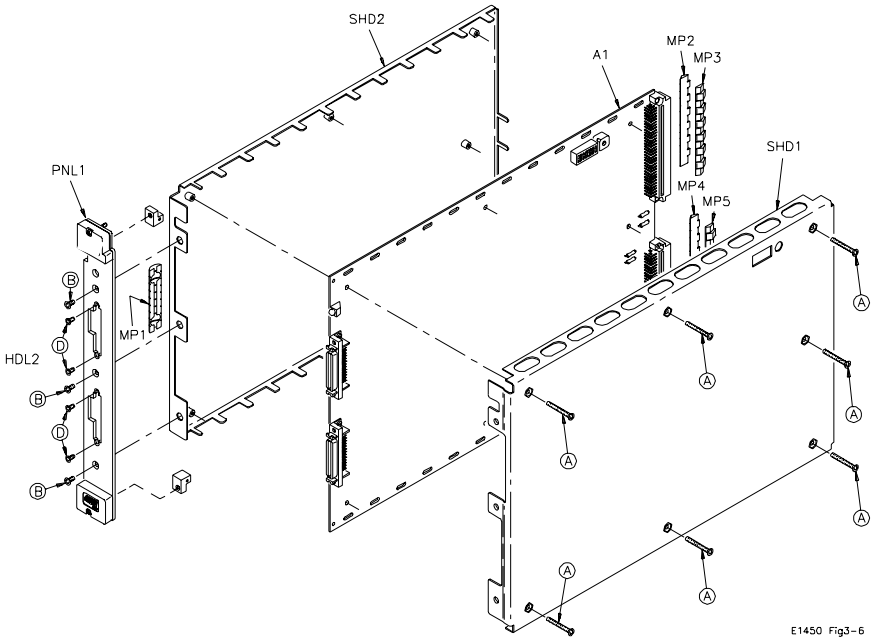

Figure 3-6. E1451A Pattern I/O Module - Hardware

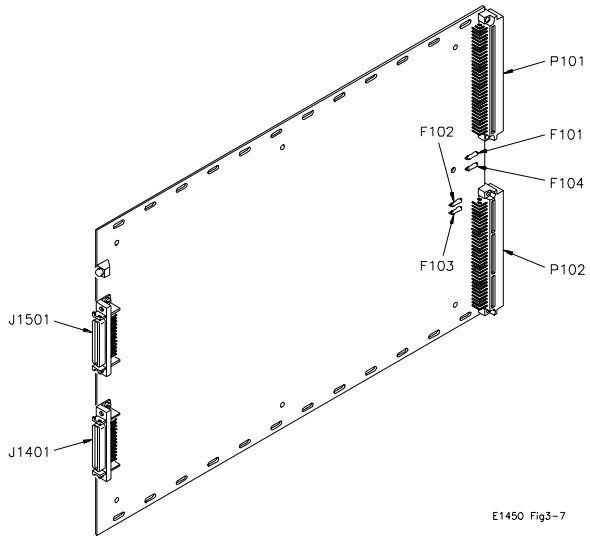

Figure 3-7. E1451A Pattern I/O Module - A1 PCA

E1451A HARDWARE PARTS LEGEND

Letter	Description	Part No.	Qty.	Reference Designation
Ⓐ	Screw	0515-1135	7	SCR1 - SCR7
Ⓑ	Screw	0515-1227	3	SCR8, SCR11, SCR12
Ⓒ	Screw Assembly	E1400-00610	2	SCR15 - SCR16
Ⓓ	Screw	0515-1375	4	SCR17 - SCR20

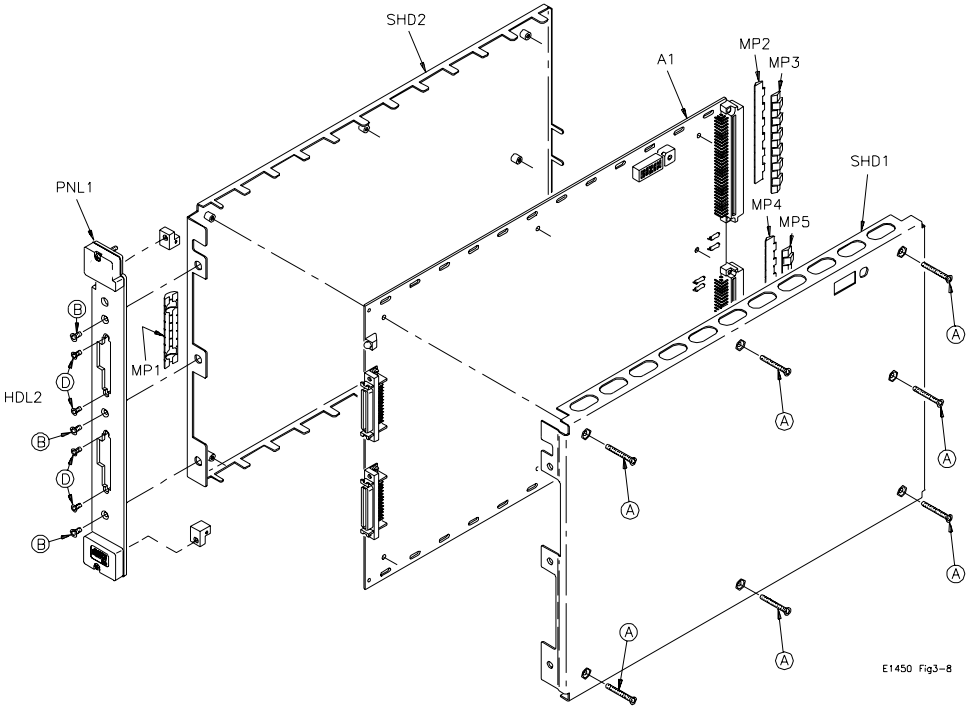

Figure 3-8. E1452A Term Patt I/O Pod - Hardware

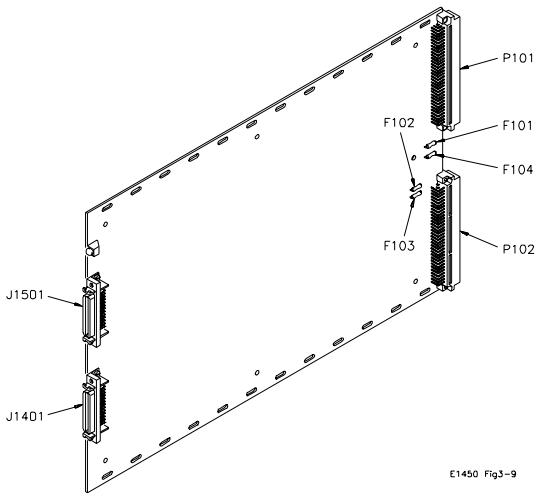

Figure 3-9. E1452A Term Patt I/O Pod - A1 PCA

E1453A HARDWARE PARTS LEGEND

Letter	Description	Part No.	Qty.	Reference Designation
Ⓐ	SCREW	0624-0600	2	SCR1 - SCR2
Ⓑ	SCREW	0624-0697	4	SCR3 - SCR6

NOTE: Insert foil (MP1, MP1A) between jacket and cable (Top and Bottom)

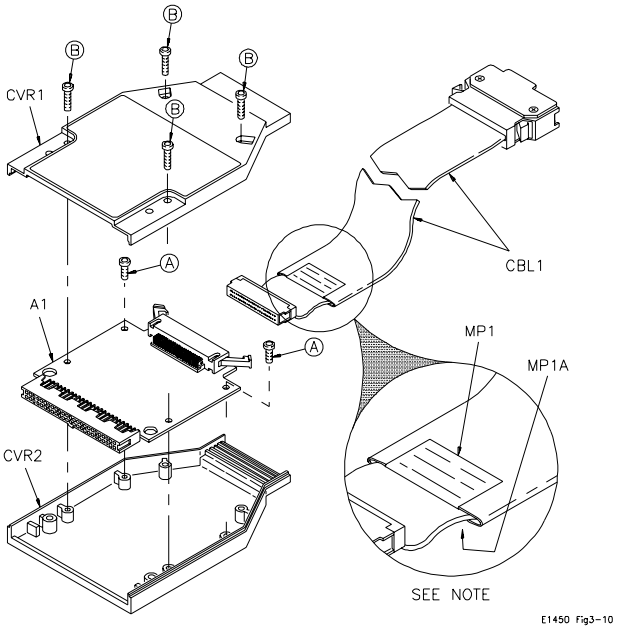

Figure 3-10. E1453A Timing Pod - Hardware Parts

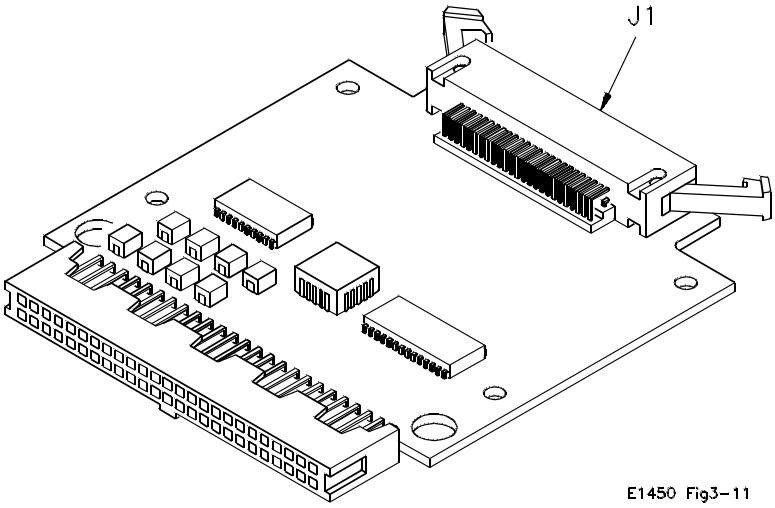

Figure 3-11. E1453A Timing Pod - A1 PCA

E1454A HARDWARE PARTS LEGEND

Letter	Description	Part No.	Qty.	Reference Designation
Ⓐ	SCREW	0624-0600	2	SCR1 - SCR2
Ⓑ	SCREW	0624-0697	4	SCR3 - SCR6

NOTE: Insert foil (MP1, MP1A) between jacket and cable (Top and Bottom)

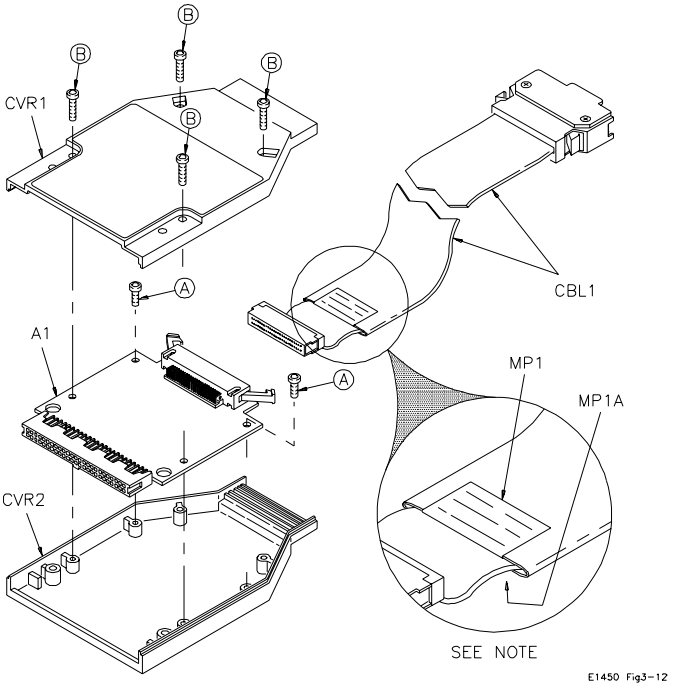

Figure 3-12. E1454A Pattern I/O Pod - Hardware Parts

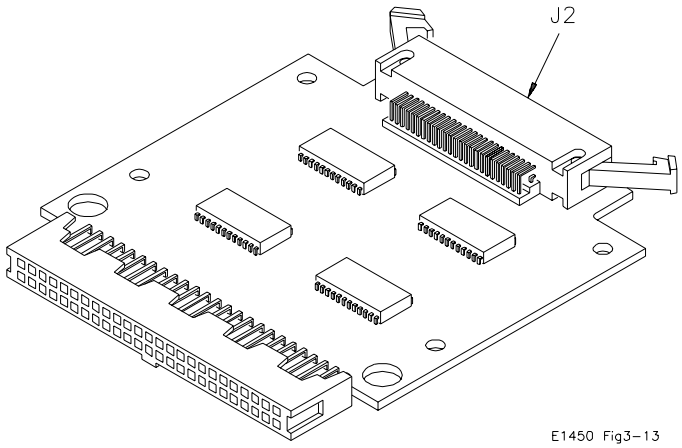

Figure 3-13. E1454A Pattern I/O Pod - A1 PCA

E1455A HARDWARE PARTS LEGEND

Letter	Description	Part No.	Qty.	Reference Designation
Ⓐ	SCREW	0515-2032	6	SCR1-SCR6

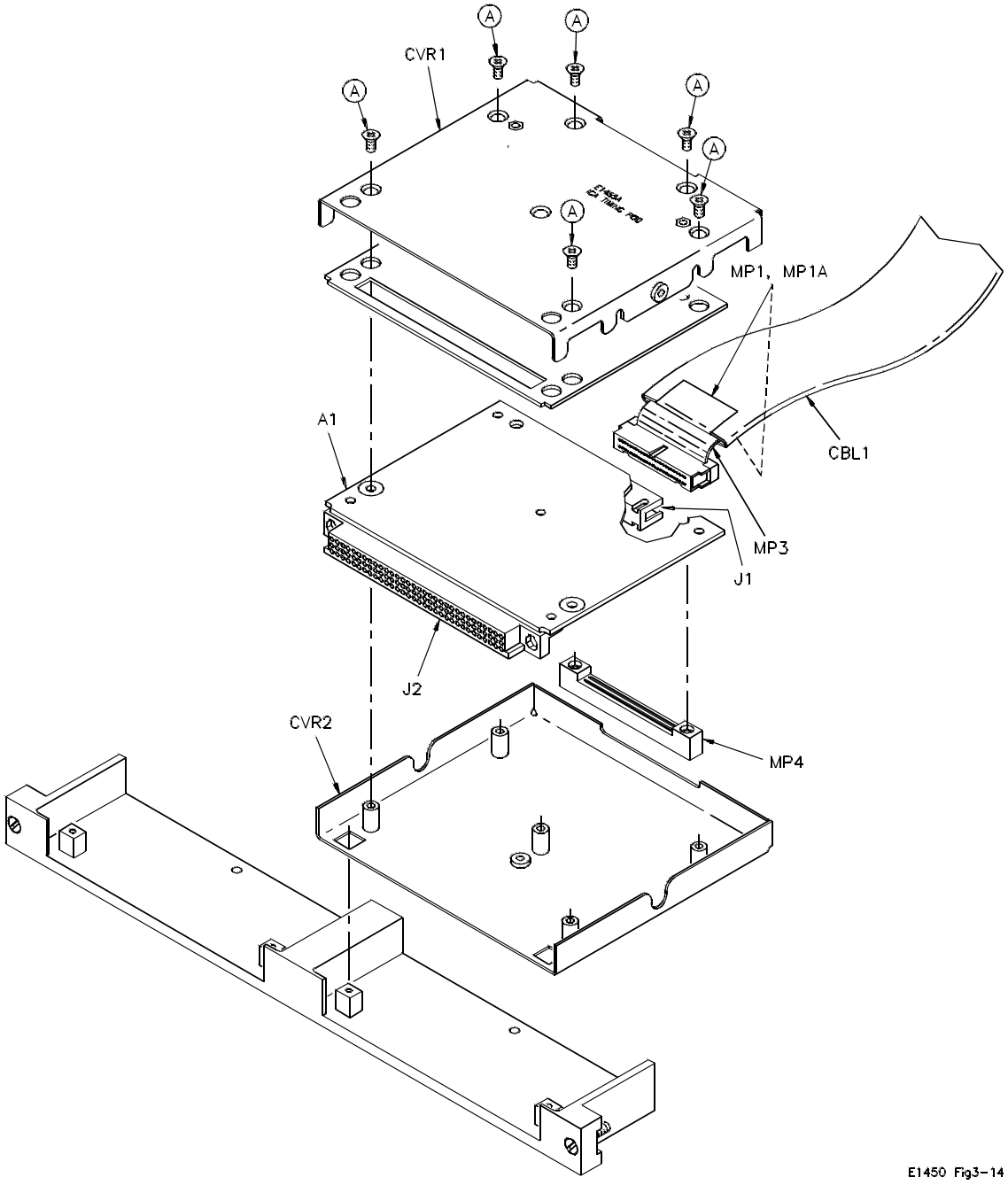

Figure 3-14. E1455A Timing Pod (MacPanel) Parts

E1456A HARDWARE PARTS LEGEND

Letter	Description	Part No.	Qty.	Reference Designation
Ⓐ	SCREW	0515-2032	6	SCR1-SCR6

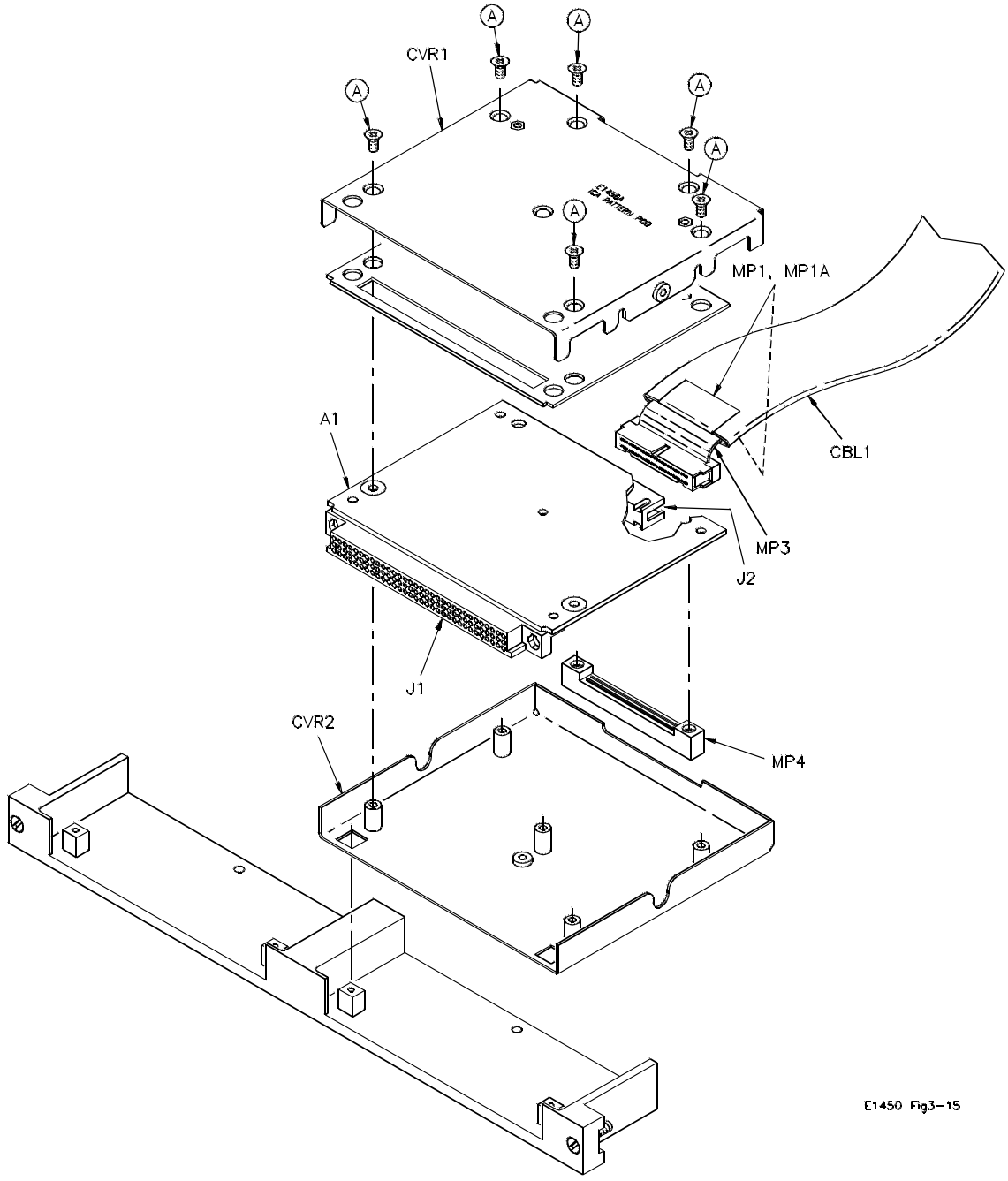

Figure 3-15. E1456A Pattern I/O Pod (MacPanel) Parts

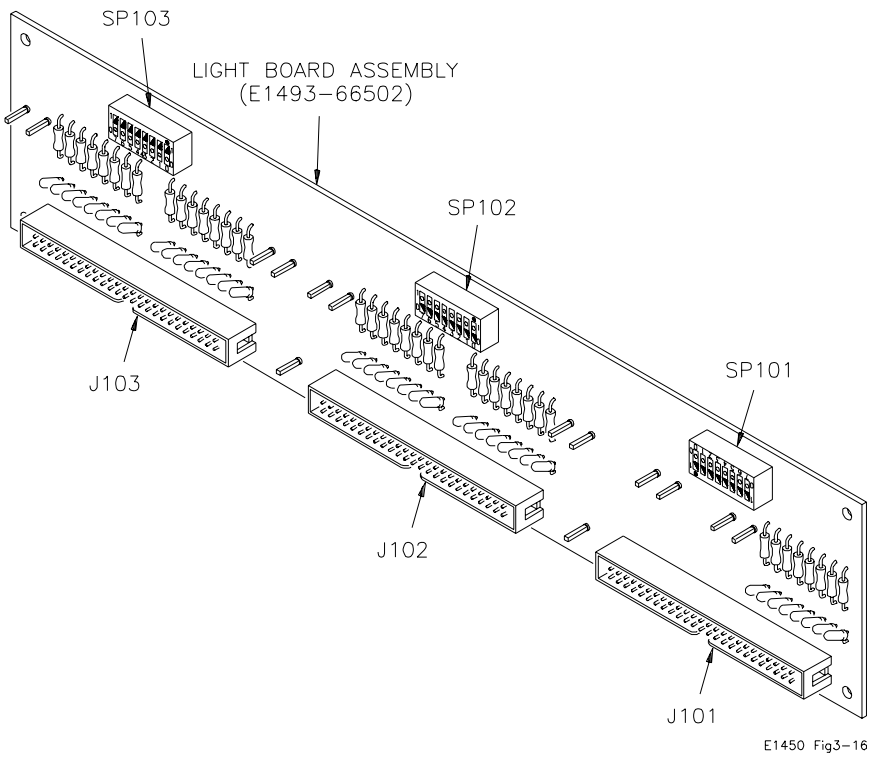

Figure 3-16. E1493A Light Board - Hardware Parts

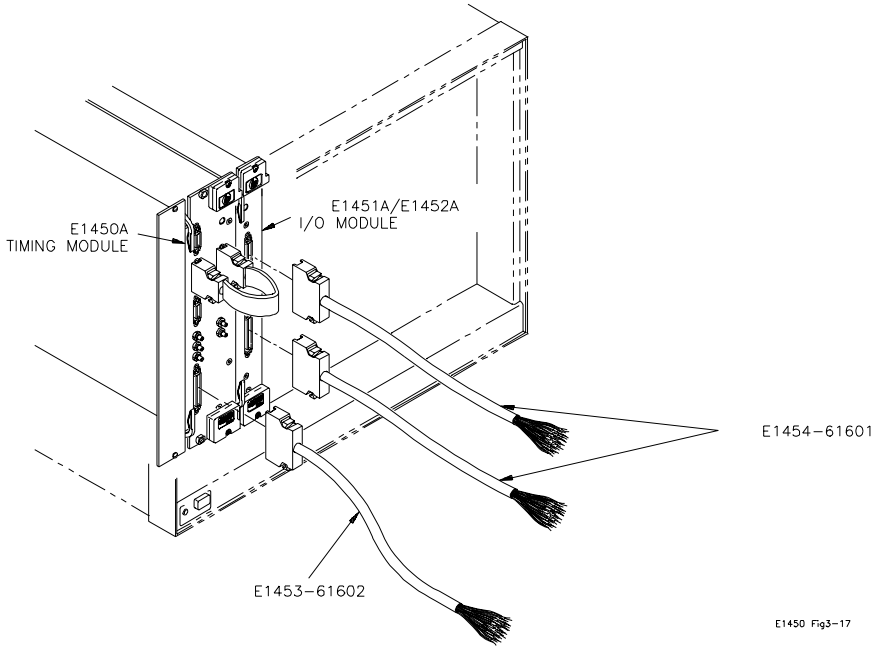

Figure 3-17. E1450A/51A/52A Interface Cables

4
Service

Introduction

This chapter contains information to service the Model D20, including:

- recommended repair strategy
- troubleshooting guidelines
- assembly/disassembly instructions
- repair/maintenance guidelines

WARNING

Do not perform any of the service procedures shown unless you are a qualified, service-trained person, and have read the WARNINGS and CAUTIONS in Chapter 1.

Equipment Required

Equipment required for Model D20 troubleshooting and repair is listed in Table 1-2, *Model D20 Recommended Test Equipment*.

Service Aids

Service aids on printed circuit boards include pin numbers, some reference designations, and assembly part numbers. See *Chapter 3 - Replaceable Parts* for descriptions and location of Model D20 replaceable parts. Service notes, manual updates, and service literature for the Model D20 may be available through Agilent Technologies.

Recommended Repair Strategy

Table 4-1 lists recommended repair strategy for Model D20 modules/pods, including the:

- Agilent E1450A Timing Module
- Agilent E1451A Pattern I/O Module
- Agilent E1452A Terminating Pattern I/O Module
- Agilent E1453A Timing Module Pod
- Agilent E1454A Pattern I/O Pod
- Agilent E1455A Timing Module Pod (Mac Panel)
- Agilent E1456A Pattern I/O Pod (Mac Panel)

Table 4-1. Model D20 Recommended Repair Strategy

Modules/Pods	Repair Strategy	Replacement Part #
Agilent E1450A Timing Module	[1] Make sure module logical address switch settings are correct. [2] Make sure module is addressed correctly by the software. [3] If [1] - [2] are ok, try the module in another slot. [4] If the module does not work in another slot, check/replace module fuses as required. Then, retest the module. [5] If [1] - [4] do not work, order a new or exch module.*	E1450-69201 (Exchange) E1450-66201 (Replacement)
Agilent E1451A/E1452A Pattern I/O Modules	[1] Make sure module logical address switch settings are correct. [2] If setting is ok, try the module in another slot. [3] If the module does not work in another slot, check/replace module fuses as required. Retest module. [4] If [1] - [3] do not work, order a new or exch module.	E1451-69201 (Exchange) E1451-66201 (Replacement) E1452-69201 (Exchange) E1452-66201 (Replacement)
Agilent E1453A/E1455A Timing Pods	Must be tested with Agilent E1450A Timing Module. If a known good pod is available, replace defective pod with good pod and check. Repairs will be limited to replacement of the PC assembly within the pod or to the cable between the pod and the E1450A Timing Module.	E1453-66501 (Pod PCA) E1453-61603 (50-pin cable) E1455-66501 (Pod PCA)
Agilent E1454A/E1456A Pattern I/O Pods	Must be tested with Agilent E1451A/52A Pattern I/O Module. If a known good pod is available, replace defective pod with good pod and check. Repairs will be limited to replacement of the PC assembly within the pod or to the cable between the pod and the E1451A/52A Pattern I/O Module.	E1454-66501 (Pod PCA) E1454-61602 (50-pin cable) E1456-66501 (Pod PCA)

* = If the above steps do not work and a known good Timing Module is available, insert the module into the mainframe and test. If the test fails, check for mainframe/backplane problems.

Troubleshooting Guidelines

This section shows suggested steps to troubleshoot Model D20 faults to a user-replaceable part on a Timing Module or Pattern I/O Module. The troubleshooting tests/checks in this chapter are designed to isolate a Model D20 fault to a fuse . If the fault cannot be traced to a fuse, return the module or pod to Agilent Technologies. See *Table 4-1 and see Chapter 3 - Replaceable Parts* for guidelines and procedures.

Troubleshooting Flowchart

Figure 4-1 shows suggested steps to troubleshoot Model D20 problems to a fuse and/or connector on the Timing Module or on an I/O module. An example program, listed in the "Service Program" section, can be used to check the Model D20.

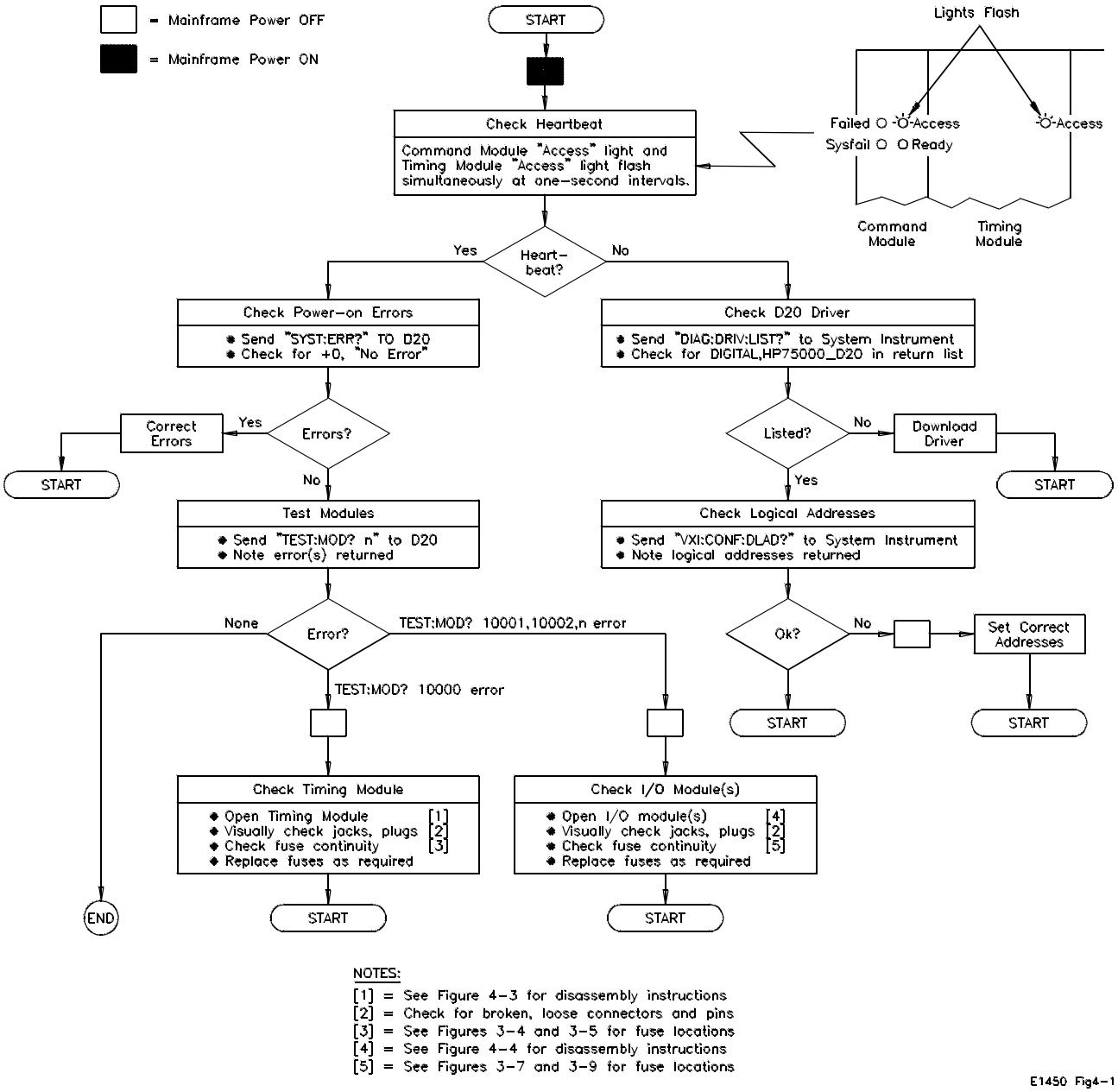

Figure 4-1. Model D20 Troubleshooting Guidelines

Service Program

This program shows one way to perform troubleshooting tests on the Model D20, using the sequence in Figure 4-1. If you want to run this program, load the "SERV_TEST" file from the Model D20 Service Programs Disk, press RUN, and follow the instructions.

NOTE

If the program will not run, check fuse F1501 on the Timing Module or fuse F101 on the I/O module(s).

```
1!    RE-STORE "SERV_TEST"
2     ! .....................................................Model D20, Command Module assignments .....................
10  Start:    !
20     ASSIGN @Syst TO 70900                                    !Assign 70900 to System Instrument
30     ASSIGN @Dft TO 70917                                     !Assign 70917 to Model D20
40     DIM Dvr_list$[100],Msg$[100]
50     DISP CHR$(129)                                           !Set display inverse video
60     OUTPUT @Dft;"*CLS"                                       !Clear D20 status register
70     CLEAR SCREEN
71     ! .....................................................Make initial setup ..........................................
80     PRINT "Model D20 Troubleshooting Guidelines"
90     PRINT
100    PRINT "  1. Turn mainframe power OFF "
110    PRINT "  2. Remove all NON-Model D20 modules from mainframe"
120    PRINT "  3. Turn mainframe power ON "
130    DISP " Press Continue when ready "
140    PAUSE
150    CLEAR SCREEN
151    ! ..............................Check Model D20 "heartbeat"  ..................................................
160    PRINT " Check Heartbeat"
170    PRINT
180    PRINT " If the Command Module and Timing Module ""Access"" lights"
190    PRINT " lights flash simultaneously at approximate one-second"
200    PRINT " intervals, the Model D20 is defined to have a ""heartbeat""."
210    INPUT " Is the heartbeat present (Y/N)? ",Hb$
220    IF Hb$="Y" OR Hb$="y" THEN Pwr_on                        !If heartbeat, check for power-on errors
221   ! ..................................................... Check Driver List  ..................................................
230   OUTPUT @Syst;"DIAG:DRIV:LIST?"                           !Query downloaded driver list
240    ENTER @Syst;Dvr_list$                                    !Enter driver list
```

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```
250  CLEAR SCREEN
260  PRINT "Check D20 Driver"
270  PRINT
280  PRINT Dvr_list$
290  INPUT " Is DIGITAL,HP75000_D20 in driver list (Y/N)? ",Dvr$
300  IF Dvr$="N" OR Dvr$="n" THEN Down_load          !If D20 driver NOT present, load driver
                                                     and rerun program
301  ! .....Check Logical Addresses .....
310  OUTPUT @Syst;"VXI:CONF:DLAD?"                   !Check logical addresses
320  ENTER @Syst;Log_addr$                           !Enter logical addresses
330  CLEAR SCREEN
340  PRINT "Check Logical Addresses"
350  PRINT
360  PRINT Log_addr$                                 !Display logical addresses
370  PRINT
380  INPUT " Are Logical Addresses correct (Y/N)? ",Addr_corr$
390  IF Addr_corr$="N" OR Addr_corr$="n" THEN Address !If addresses incorrect, fix and rerun
                                                     program
400  GOTO Start                                      !If addresses are ok, rerun program
                                                     from start
401  ! .....Check Power-On Errors.....
410 Pwr_on:   !                                      !Checks for power-on errors
420  CLEAR SCREEN
430  PRINT "Check Power-on Errors"
440  PRINT
450  REPEAT
460    OUTPUT @Dft;"SYST:ERR?"                       !Queries errors until +0 appears
470    ENTER @Dft;Msg$
480    PRINT Msg$                                    !Display system errors
490  UNTIL Code=0
500  INPUT " Any power-on errors (Y/N)? ",Pwr_on_tst$
510  IF Pwr_on_tst$="Y" OR Pwr_on_tst$="y" THEN End_test_pwr   !If there are errors, correct and rerun
                                                     program
511  ! .....Test modules (TEST:MOD? n) .....
520  OUTPUT @Syst;"VXI:CONF:DNUM?"                   !Check number of modules installed
530  ENTER @Syst;Nbr_mods                            !Enter number of modules
540  CLEAR SCREEN
550  PRINT "Test Modules"
560  PRINT
570   FOR I=O TO Nbr_mods-2
```

(continued on next page)

```
580       OUTPUT @Dft;"TEST:MOD? ";I                    !Test each installed module
590       ENTER @Dft;Mod_err$(I)                        !Enter module error code
600       PRINT "Module";I;"= ";Mod_err$(I)             !Display module error code
610    NEXT I                                           !Next module
620    PRINT
630    PRINT "+0,+0,+0,+0 returned indicates no error for the module."
640    PRINT "If there are any error messages, note the module NUMBER(S)"
650    PRINT "for the error messages."
660    INPUT " Any error messages (Y/N)? ",Err_msg$
670    IF Err_msg$="N" OR Err_msg$="n" THEN End_test  !End program if no module errors
680    INPUT " Enter number (0,1,2,...) of FIRST module with error message ",Err_num
690    IF Err_num>0 THEN Io_mod                       !If first module error = 0, test Timing
                                                      Module
691    ! .....Timing Module Checks .....
700  Tim_mod:  !
710    CLEAR SCREEN
720    PRINT "Check Timing Module"
730    PRINT
740    PRINT "  1. Turn mainframe power OFF"
750    PRINT "  2. Remove Timing Module from mainframe "
760    PRINT "  3. Disassemble Timing Module (see Fig 4-3)"
770    PRINT "  4. Inspect jacks/plugs for broken/bad connections"
780    PRINT
790    PRINT "  5. Check fuses F1501, F1502, F1503 on A1 PCA (see Fig 3-3)"
800    PRINT "  6. Check fuses F1401, F1402, F1403 on A2 PCA (see Fig 3-4)"
810    PRINT "  7. Replace fuses as necessary "
820    PRINT "  8. Reassemble Timing Module"
830    PRINT
840    PRINT "  9. Reinstall module in mainframe"
850    PRINT " 10. Turn mainframe power ON"
860    PRINT " 11. When ready, press Continue to rerun this program"!Re-check Model D20 after repair
870    PAUSE
880    CLEAR SCREEN
890    GOTO Start
891    ! .....Pattern I/O Module Checks .....
900  Io_mod:  !                                       !Check first I/O module with error code
910    INPUT " Enter the number of the FIRST I/O module with error ",Io_num
920    CLEAR SCREEN
930    PRINT "Check I/O Module Number";Io_num
```

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```
940   PRINT
950   PRINT "    1. Turn mainframe power OFF"
960   PRINT "    2. Remove I/O module from mainframe "
970   PRINT "    3. Disassemble I/O module (see Fig 4-4)"
980   PRINT
990   PRINT "   4. Inspect jacks/plugs for broken/bad connections"
1000  PRINT "   5. Check fuses F101, F102, F103, and F104 on A1 PCA (see Fig 3-7)"
1010  PRINT "   6. Replace fuses as necessary "
1020  PRINT
1030  PRINT "   7. Reassemble I/O module"
1040  PRINT "   8. Reinstall module in mainframe"
1050  PRINT "   9. Turn mainframe power ON"
1060  PRINT "  10. When ready, press Continue to rerun this program"!Re-check Model D20 after repair
1070  PAUSE
1080  CLEAR SCREEN
1090  GOTO Start
1100 End_test_pwr: !                                    !Instructions to correct power-on errors
1110  CLEAR SCREEN
1120  PRINT
1130  PRINT "If there are are power-on errors:"
1140  PRINT
1150  PRINT "   1. Exit this program "
1160  PRINT "   2. Correct the errors "
1170  PRINT "   3. Rerun this program "
1180  STOP
1181 ! .....Downloading Driver instructions.....
1190 Down_load:  !                                      !Instructions to download D20 driver
1200  CLEAR SCREEN
1210  PRINT " The Model D20 driver is not installed"
1220  PRINT
1230  PRINT "    1. Exit this program"
1240  PRINT "    2. Install Model D20 driver (see Model D20"
1250  PRINT "       SCPI Driver Installation Note)"
1260  PRINT "    3. Rerun this program "
1270  STOP
1271  ! .....Setting Logical Address instructions .....
1280 Address:  !
1290  CLEAR SCREEN
```

(continued on next page)

```
1300  PRINT " To set correct logical addresses:"
1310  PRINT
1320  PRINT "    1. Turn mainframe power OFF"
1330  PRINT "    2. Remove module(s) with wrong address"
1340  PRINT "    3. Set correct addresses (See Model D20 "
1350  PRINT "       Hardware Installation Guide)"
1360  PRINT
1370  PRINT "    4. Reinstall modules"
1380  PRINT "    5. Turn power ON"
1390  PRINT "    6. When ready, press Continue to rerun this program"
1400  PAUSE
1410  GOTO Start
1420 End_test:  !
1430  CLEAR SCREEN
1440  PRINT "This completes the Model D20 troubleshooting tests"
1450  END
```

Typical Results

If the Model D20 is operating properly, the following results are *typical* for a Model D20 consisting of a Timing Module (module 0) and a Terminating Pattern I/O Module (module 1).

```
Check Power-On Errors
+0,"No error"

Test Modules
Module 0 = +0, +0, +0,+0
Module 1 = +0, +0, +0,+0

Check D20 Driver
DIGITAL,HP75000_D20,A.01.00,RAM;SYSTEM,E1405B,A.08.01,
ROM;UNKNOWN,UNKNOWN,0,ROM;VOLTMTR,E1326B,A.01

Check Logical Addresses
+0,+136,+137
```

Assembly/ Disassembly Instructions

This section shows how to disassemble and reassemble the Agilent E1450A Timing Module, the Agilent E1451A Pattern I/O Module, and the Agilent E1452A Terminating Pattern I/O Module. See Figure 3-10 for Timing Pod disassembly or Figure 3-12 for Pattern I/O Pod disassembly.

CAUTION

Do not handle or disassemble Model D20 modules unless you are familiar with the precautions listed in the "Repair/Maintenance Guidelines" section of this chapter.

Preparing Modules for Disassembly

See Figure 4-2 to prepare Model D20 modules for disassembly. To perform disassemblies, you will need a T-10 Torx driver, a T-8 Torx driver, and a 1/4-inch hex nut driver.

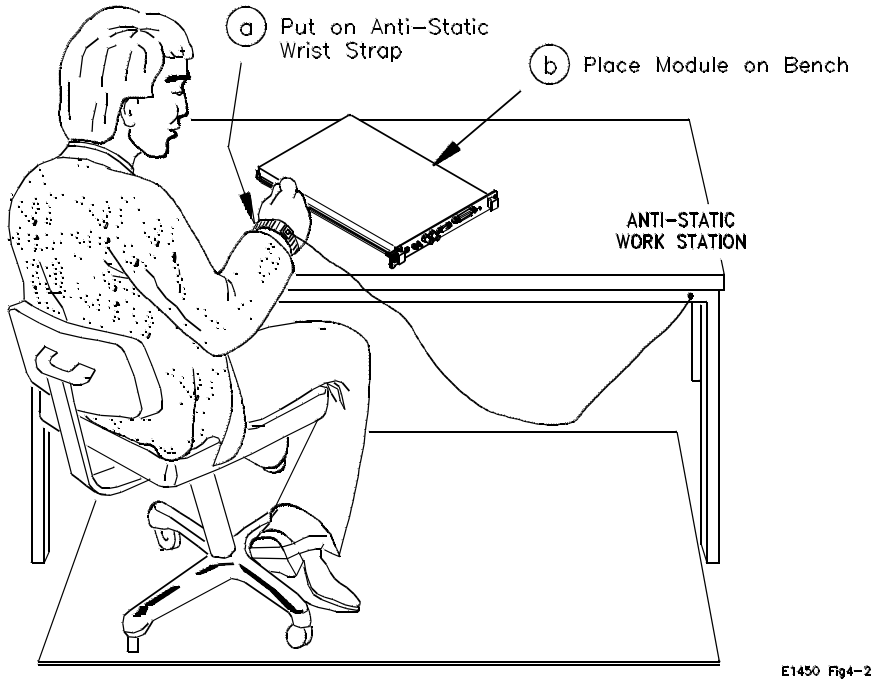


Figure 4-2. Preparing Modules for Disassembly

Timing Module Disassembly

See Figure 4-3 to disassemble the Agilent E1450A Timing Module cover, A1 PCA, and A2 PCA. Reverse the steps shown to reassemble the Timing Module and PCAs.

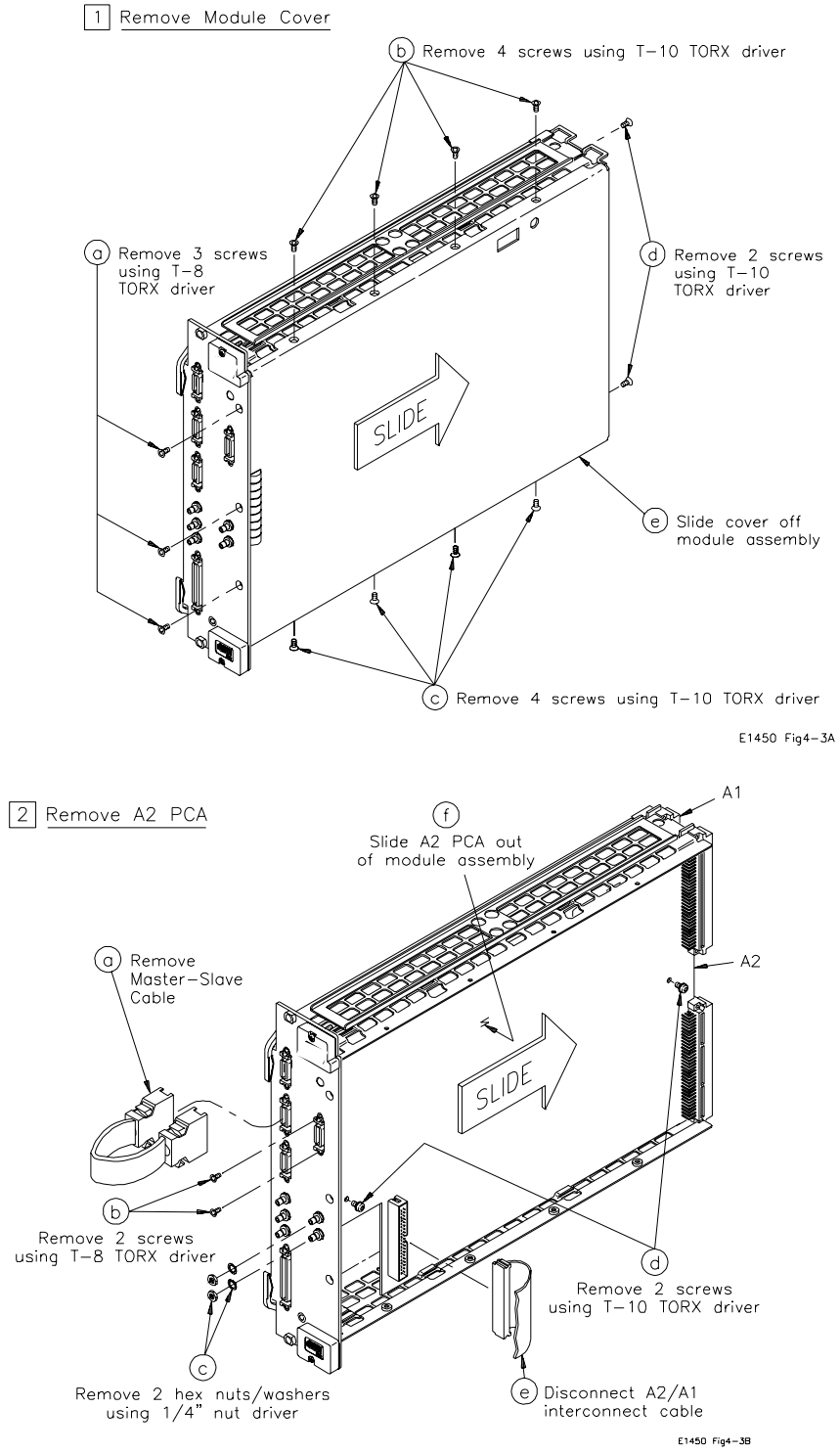


Figure 4-3. Timing Module Disassembly

(continued on next page)

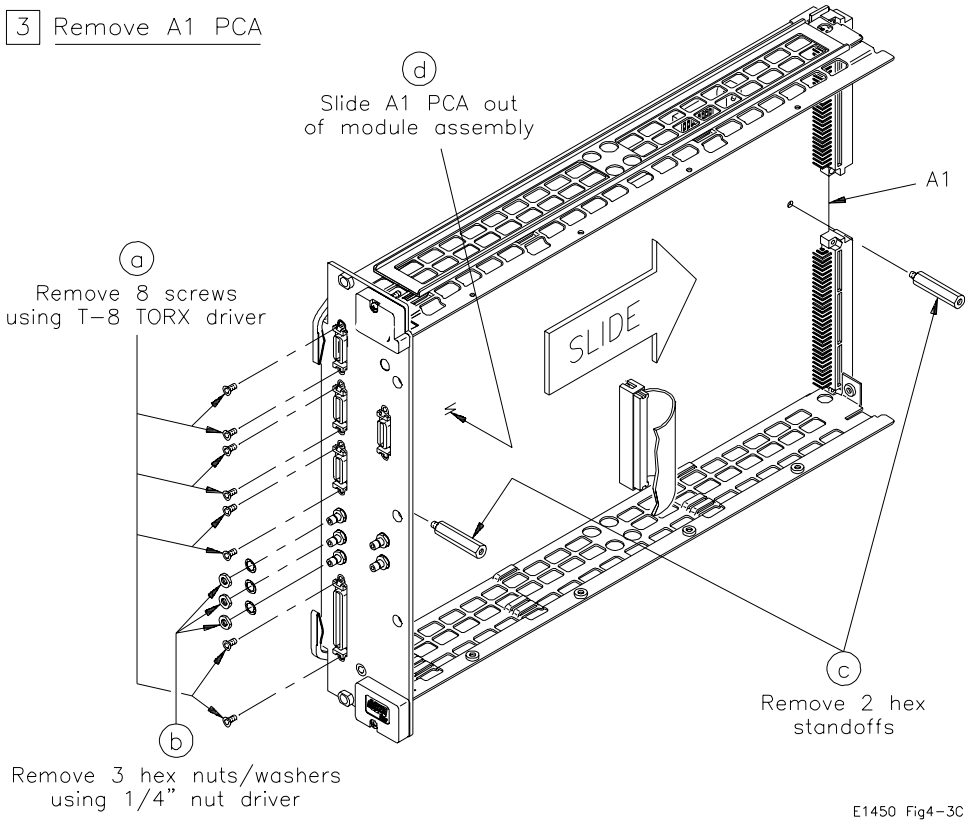
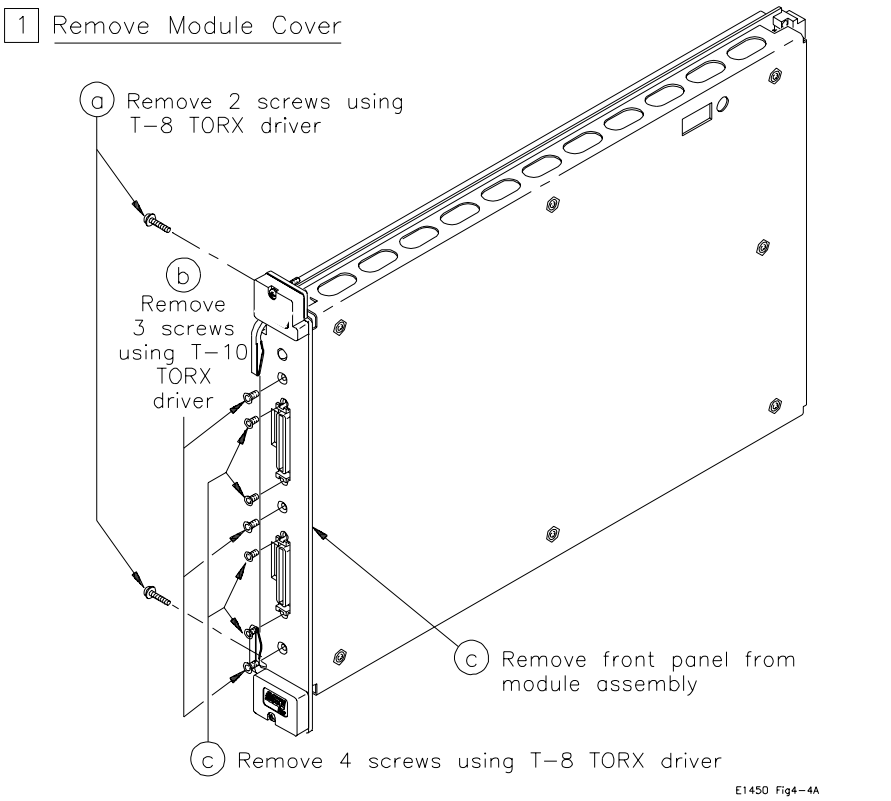


Figure 4-3 (cont'd). Timing Module Disassembly

Pattern I/O Modules Disassembly

See Figure 4-4 to disassemble the Agilent E1451A/52A Pattern I/O Module cover and A1 PCA. Reverse the steps shown to reassemble the Pattern I/O Module and PCA.



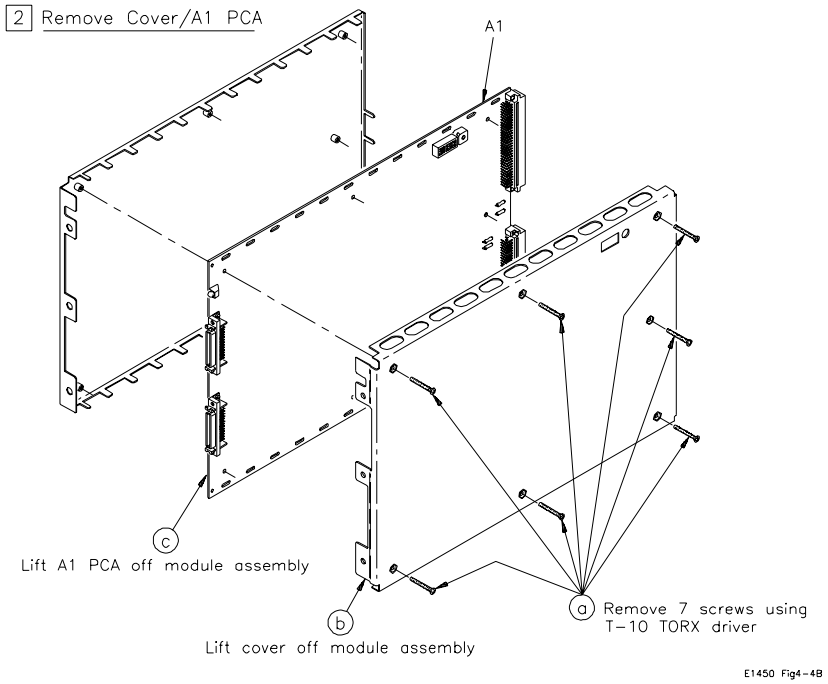


Figure 4-4. Pattern I/O Modules Disassembly

Repair/ Maintenance Guidelines

Guidelines to repair and maintain Model D20 modules follow, including:

- ESD precautions
- Soldering printed circuit boards
- Post-repair safety checks

ESD Precautions

Electrostatic discharge (ESD) may damage CMOS and other static-sensitive devices in Model D20 modules. This damage can range from slight parameter degradation to catastrophic failure. When handling Model D20 modules, follow these guidelines to avoid damaging components:

- Always use a static-free work station with a pad of conductive rubber or similar material when handling Model D20 components.
- After you remove a module from the frame, place the module on a conductive surface to guard against ESD damage.
- Do not use pliers to remove a CMOS device from a high-grip socket. Instead, use a small screwdriver to pry the device up from one end. Slowly lift the device up, one pair of pins at a time.
- After you remove a CMOS device from a module, place the device onto a pad of conductive foam or other suitable holding material.
- If a device requires soldering, be sure the device is placed on a pad of conductive material. Also, be sure you, the pad, and the soldering iron tip are grounded to the device. Apply as little heat as possible when soldering.

Soldering Printed Circuit Boards

The etched circuit boards on Model D20 printed circuit assemblies (PCAs) have plated-through holes that allow a solder path to both sides of the insulating material. Soldering can be done from either side of the board with equally good results. When soldering to any circuit board, keep in mind the following guidelines:

CAUTION

Do not use a sharp metal object such as an awl or twist drill, since sharp objects may damage the plated-through conductor.

- Avoid unnecessary component unsoldering and soldering. Excessive replacement can result in damage to the circuit board and/or adjacent components.
- Do not use a high power soldering iron on etched circuit boards, as excessive heat may lift a conductor or damage the board.
- Use a suction device or wooden toothpick to remove solder from component mounting holes. When using a suction device, be sure the equipment is properly grounded to prevent electrostatic discharge from damaging CMOS devices.

Post-Repair Safety Checks

After making repairs to Model D20 components, inspect the device for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine and correct the cause of the condition. Then, run the self-test (*TST?) command to verify that the Model D20 is operational.

NOTE

As desired, you may want to run one or more of the functional and/or performance verification tests in Chapter 2 - Verification Tests.

5
DIAGnostic Commands

Introduction

This chapter describes the DIAGnostic commands subsystem for use in servicing the Agilent 75000 Model D20. See *Chapter 4 - Command Reference* in the *Model D20 Task and Command Reference* for a description of command types, formats, and syntax.

Some DIAGnostic commands bypass normal instrument functions and can cause unpredictable results when combined with normal commands. See Table 5-1 for DIAGnostic command subsystem summaries.

Table 5-1. DIAGnostic Subsystem Descriptions

DIAGnostic subsystem	Description
:OSCillator [:STATe]1|0|ON|OFF [:STATe]?	Allows synchronization between Model D20s in different VXI mainframes. Enables or disables the Timing Module oscillator.
:REGister [:VALue]<module_#>,<register>,<value> [:VALue]?<module_#>,<register>	Sets the value or queries the value held by a hardware register in an instrument module.
:SEQuence :LOOP :BOUNdary <begin_vector>,<end_vector> :BOUNDary? [:STATe] 1|0|ON|OFF [:STATe]?	DIAGnostic:SEQuence:LOOP allows a looping capability on the currently selected DIGital:SEQuence.
:SEQuence :MEMory :ATTRibute <module_#>,<port>,<seq_addr>,<block> :ATTRibute? <module_#>,<port>,<seq_addr>,<count> [:COMBined] <module_#>,<port>,<seq_addr>,<block> [:COMBined]? <module_#>,<port>,<seq_addr>,<count> :DATA <module_#>,<port>,<seq_addr>,<block> :DATA? <module_#>,<port>,<seq_addr>,<count>	DIAGnostic:SEQuence:MEMory uses special, high-speed GPIB transfers to load and read attribute and/or data information directly to and from the instrument hardware.
:SYSTem :HEALth :CHECk 1|0|ON|OFF :CHECk? [:STATus]?	Enables or disables consideration of port "health" when forming a pin group. Returns status information for each module in the Model D20.
:TIMing :VALid?<start_vector>	Returns problems found on the currently selected TIMing:CYCLe:SEQuence.

DIAGnostic: OSCillator

The **DIAGnostic:OSCillator** subsystem enables or disables the oscillator in the Timing Module. A primary function for DIAGnostic:OSCillator is to enable synchronization between Model D20s in different VXI mainframes.

CAUTION

Turning off the master oscillator in the Timing Module can cause a failure of subsequent commands meant to modify the state of the Timing Module. The oscillator should be turned off only during the synchronization process.

Subsystem Syntax

DIAGnostic:OSCillator subsystem	Description
:OSCillator [:STATe] 1|0|ON|OFF [:STATe]?	 Enables/disables Timing Module oscillator Queries *master* Timing Module oscillator state

DIAGnostic:OSCillator[:STATe]

Description

DIAGnostic:OSCillator[:STATe] *1|0|ON|OFF* enables or disables the oscillator in the master Timing Module.

DIAGnostic:OSCillator[:STATe]? returns the state of the master Timing Module oscillator: enabled (1) or disabled (0).

Parameters

Parameter Name	Parameter Type	Range of Values
1|0|ON|OFF	numeric NR1| discrete	1|0|ON|OFF (ON or OFF can be used instead of 1 or 0). 1 or ON enables the oscillator, 0 or OFF disables oscillator.

Comments

- **Synchronization Requirements:** [:STATe] is set to ON (1) at power-on and after *RST. Requirements for synchronization are that all timing modules are tied to the same master section and programmed identically.

- **Synchronize Sequence Start:** Synchronize the start of a sequence run as follows:
  - Disable the master timing module oscillator
  - Send RUN commands to all D20s
  - Enable master timing oscillator to begin synchronized operation

---

NOTE

For MXI, this procedure is necessary ONLY for driver revision A.01.0x OR if all modules have NOT been combined into a single instrument.

- **GPIB Expansion:** For multiple mainframe operation using GPIB expansion, an Agilent E1405 Command Module is required in each slave mainframe, and a Command Module is required in the master mainframe (see Figure 5-1).
- **MXIbus Expansion**: For multiple mainframe operation using MXIbus (Agilent E1482A Extender) expansion, an Agilent E1405/E1406 Command Module is required in the master mainframe and an Agilent E1482A Extender is required in EACH mainframe (see Figure 5-1).

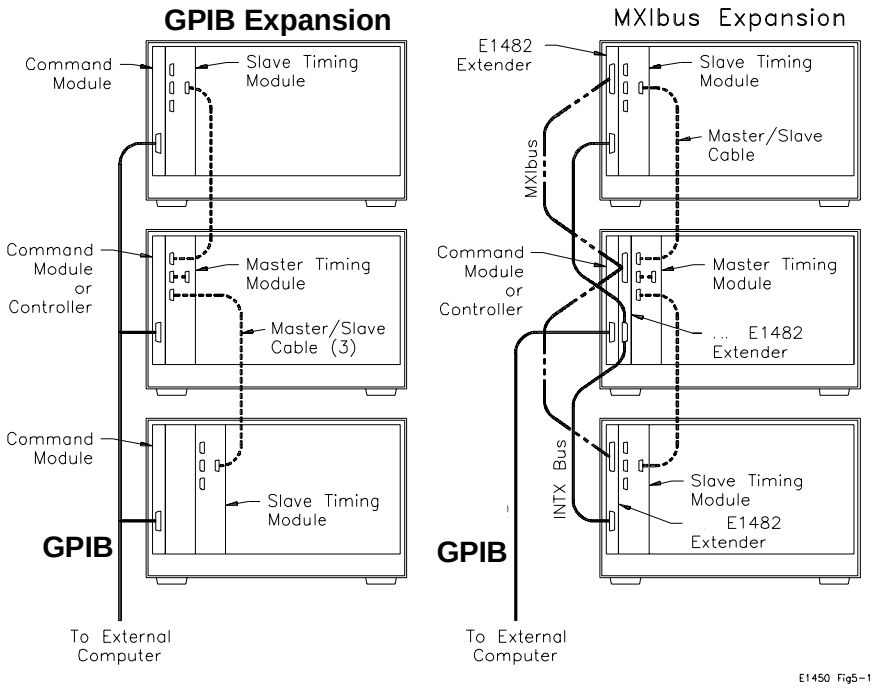


Figure 5-1. Typical GPIB/MXIbus Expansions

Example Program

This example shows one way to use the DIAG:OSC[:STAT] command and GPIB expansion to synchronize the start of a sequence. The Model D20 at address 70902 is the master and Model D20s at addresses 70903 and 70904 are the slaves. See Figure 5-1 for typical connections.

```
1   !Example: Synchronized Operation
2   !
3   !---------- Set up Sequences and Patterns ----------
                    .
                    .
109  !---------- Disable master Timing Module Oscillator ----------
110  OUTPUT 70902;"DIAG:OSC OFF"                    !Disable master oscillator
111  ! ----------Issue RUN commands to all oscillators ----------
120  OUTPUT 70902;"RUN"                             !RUN to master
130  OUTPUT 70903;"RUN"                             !RUN to slave #1
140   OUTPUT 70904;"RUN"                            !RUN to slave #2
161  ! ---------- Enable master Timing Module oscillator ----------
170   OUTPUT 70902;"DIAG:OSC ON"                    !Enable master oscillator
171  !---------- Synchronized Operation Begins ----------
180   END
```

DIAGnostic: REGister

The **DIAGnostic:REGister** subsystem sets the value or queries the value held by a hardware register on one of the modules in the Model D20 instrument.

Subsystem Syntax

DIAGnostic:REGister Subsystem	Description
:REGister [:VALue] <module_#>,<register>,<value> [:VAlue]? <module_#>,<register>	writes a value to specified register reads value of specified register

DIAGnostic:REGister[:VALue]

Description

DIAGnostic:REGister[:VALue]<*module_#*>,<*register*>, <*pattern_value*> sets the value held by the specified hardware register on the specified module in the Model D20 instrument.

DIAGnostic:REGister[:VALue]?<*module_#*>, <*register*> returns the current contents of the specified register on the specified module, in the format specified by the most recent FORMAT command.

Parameters

Parameter Name	Parameter Type	Range of Values
<module_#>	numeric (NRf)	0 to number of last module
<register>	numeric (NRf) |non-decimal Must be even values.	Address of the register in which the value is set.
<value>	numeric (NRf)| non-decimal	Maximum value for 16-bit register.

NOTE

NRf format is treated as an unsigned 16-bit integer. That is, its valid range is 0 - 65535 (no negative values allowed).

Comments

- **Register Addresses:** See the *Agilent E1450 Hardware Manual* for Timing Module register addresses. See the *Agilent E1451/52 Hardware Manual* for Pattern I/O Modules register addresses.
- **Register Addresses Must be Even:** The register parameter is interpreted as a byte address, but only word addresses are allowed on the hardware. Therefore, <*register*> must be an even number.
- **Base Address Automatically Added:** When using the DIAG:REG:VAL command and an Agilent E1405B Command Module, do not add the Base Address to the Register Offset to arrive at the Register Address, as shown in the *Agilent E1450 Hardware Manual* and *Agilent E1451/52 Hardware Manual.* The Base Address is automatically computed by the DIAG:REG:VAL command.

CAUTION

Do NOT write to the Timing Module Calibration ROM register (address 0E $_H$) or to any Pattern I/O Module's Calibration ROM Register (address 06 $_H$). Doing so may alter the Calibration ROM's contents, causing the module to fail and requiring factory repair.

Model D20 repairs performed by an Agilent Technologies Service Center to replace calibration constants erased by register-based programming are not covered by the product warranty.

Example Program

This program uses DIAGnostic:REGister:VALue? to read the current register value.

To RUN the following program:

- Insert *Model D20 Service Programs Disk* in disk drive
- Load DIAGnostic programs file with LOAD "DIAG_CMD"
- Press RUN
- Select "*Example: Reading Register Values*"

```
1     ! Example: Reading Register Values
2     ! ..... Make assignments .....
10    DIM A(100),B$[100],C$[100]
20    ASSIGN @Dft TO 70917
30    INPUT " Enter module number (0,1,2,...) ",Mod_num
40    IF Mod_num=0 THEN
50      Addr=46                                   !Max (dec) address for Timing Module
60    ELSE
70      Addr=62                                   !Max (dec) addr for Pattern I/O  Module
80    END IF
81    !..... Print Results .....
90  Format:IMAGE 2X,2A,8X,2D,9X,5D,8X,4A,X,4A,X,4A,X,4A
100   PRINT "Register Values for Module";Mod_num
110   PRINT
120   PRINT "Hex      Decimal    Decimal       Bit Pattern"
130   PRINT "Address  Address    Value          (15 ---- 0)"
140   PRINT
150   FOR I=0 TO Addr STEP 2
160     OUTPUT @Dft;"DIAG:REG:VAL? ";Mod_num,I  !Query module registers
170     ENTER @Dft;A(I)                         !Enter register value
180     B$=DVAL$(A(I),2)                        !Convert register values to binary string
190     C$=DVAL$(I,16)                          !Convert register addresses to Hex
200     PRINT USING Format;C$[7;8],I,A(I),B$[17,20],B$[21,24],
B$[25,28],B$[29,32]                             !Display results
210   NEXT I                                    !Next register
220   END
```

Typical Results

A typical return follows for the Timing Module assuming a TEST? command has been sent to the Model D20. The return for a Pattern I/O module is similar, except the display is up to address $3E_H$ (62 decimal).

```
Register Values for Module 0

Hex       Decimal     Decimal      Bit Pattern
Address   Address      Value        (15 ---- 0)

00          0          65535     1111 1111 1111 1111
02          2            338     0000 0001 0101 0010
 .          .             .              .
2E         46          64512     1111 1100 0000 0000
```

DIAGnostic: SEQuence: LOOP

DIAGnostic:SEQuence:LOOP allows a continuous looping capability (on the currently selected DIGital:SEQuence) useful in diagnostic situations. This looping feature is not available in the normal command set (i.e., part of the DIGital:SEQuence subsystem) because it is impossible to discover the correct order in which compare errors occurred, and the marker function cannot be used within a loop.

Subsystem Syntax

DIAGnostic:SEQuence:LOOP Subsystem	Description
:SEQuence :LOOP :BOUNdary <begin_vector>,<end_vector> :BOUNDary? [:STATe] 1|0|ON|OFF [:STATe]?	 Sets loop boundary limits Queries loop boundary limits Enables/disables looping capability Queries loop state for selected sequence

DIAGnostic:SEQuence:LOOP:BOUNdary

Description

DIAGnostic:SEQuence:LOOP:BOUNdary <*begin_vector*>, <*end_vector*> sets the boundary limits of the loop. <*end_vector*> sets the last vector executed in the loop, and <*begin_vector*> sets the first vector executed in the loop (i.e., the vector executed initially and the vector executed immediately after the <*end_vector*>) during looping.

DIAGnostic:SEQuence:LOOP:BOUNdary? queries the boundary limits of the diagnostic loop. The command response is <*begin_vector*> and <*end_vector*>.

Parameters

Parameter Name	Parameter Type	Range of Values
<begin_vector>	numeric (NRf)	0 to the last vector of the sequence - 3 (see <end_vector> requirement).
<end_vector>	numeric (NRf)	Cannot be less than <begin_vector> + 3.

Comments

- The TIMing:MARKer:SEQuence must be all set to 0s between <*begin_vector*> and <*end_vector*>. This is because the same bit that controls the marker in the Timing Module's sequence memory also controls branching.

- **Windows Affect Loops:** When a window is established (with SEQuence:WINDow), the DIAGnostic:SEQuence:LOOP:BOUNdary operation may be affected.

  For example (see Figure 5-2 (a)), the window range (vectors 3 through 12) is greater than the loop range (vectors 5 through 10). The loop sequence starts at vector 3, goes to 10 and then loops 5 through 10. However (see Figures 5-2(b) and (c)), if the window range is less than the loop range, the sequence executes through the window range ONCE and STOPS.

- **Breakpoints vs. Range:** Breakpoints (established with SEQuence:BREak) within the loop boundary behave normally. If the breakpoint is active, when its vector is executed the Model D20 will enter its PAUSed state. A CONTinue command will continue the looping until the next breakpoint is encountered.

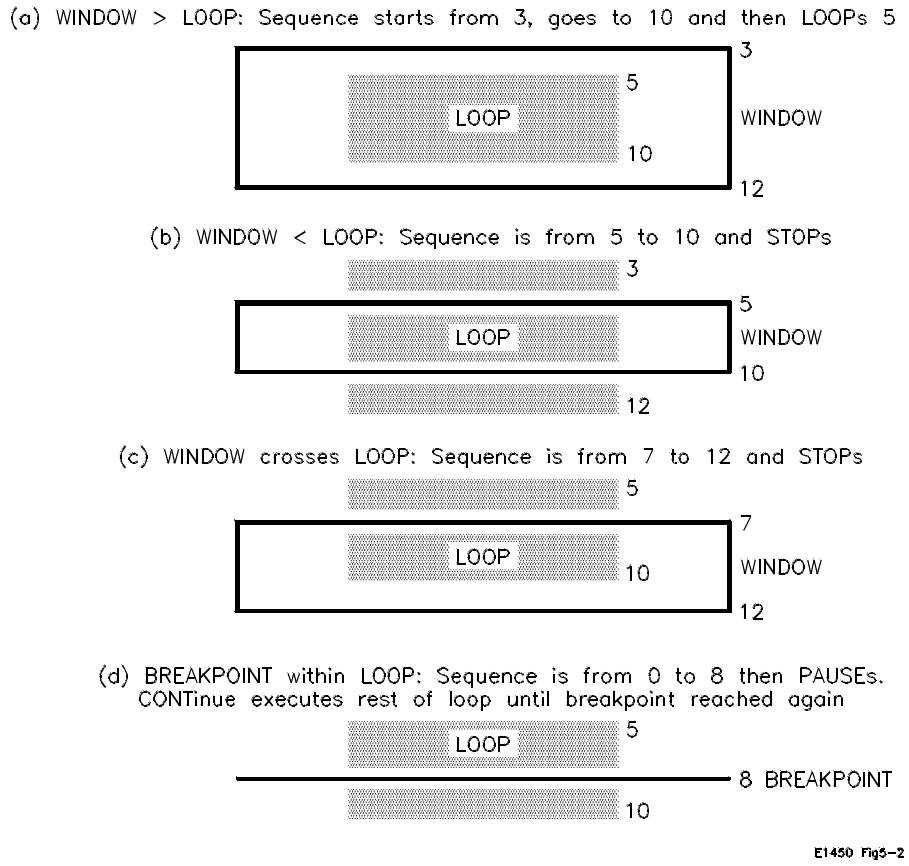


Figure 5-2. Example: LOOP vs. WINDOWS/BREAKPOINTS

Example Program

This program sets up and initiates a sequence loop and a window for sequence "TEST_1". The sequence RUNs twice. For the first RUN, the window boundaries (vectors 0 and 7) are larger than the loop boundaries (vectors 2 and 7), so the LEDs on the Light Board light sequentially from 0 through 7 and then loop from 2 through 7 for 10 seconds.

For the second RUN, the window boundaries (vectors 1 and 6) are smaller than the loop boundaries (vectors 0 and 7), so the LEDs light ONCE sequentially from 1 through 6 and the sequence stops. Then, after a 10-second delay, the instrument is reset and the program ends.

To RUN the following program:

- Insert *Model D20 Service Programs Disk* in disk drive
- Load DIAGnostic programs with LOAD "DIAG_CMD"
- Press RUN
- Select "*Example: Looping a Sequence*"

```
1   ! Example: Looping a Sequence
2   !
3   !.....Set up Sequence.....
10   ASSIGN @Dft TO 70917                                  !Assign 70917 to Model D20
20   OUTPUT @Dft;"*RST"                                    !Set instrument to known condition
30   OUTPUT @Dft;"SEQ:DEL:ALL"                             !Delete all existing sequences
40   OUTPUT @Dft;"SEQ:DEF TEST_1,9"                        !Sequence "TEST_1" has 9 vectors
50   OUTPUT @Dft;"SEQ TEST_1"                              !Select sequence "TEST_1"
51   !..... Define Pin Group.....
60   OUTPUT @Dft;"GRO:DEL:ALL"                             !Delete all existing groups
70   OUTPUT @Dft;"GRO:DEF DATA_OUT,(@1(1,0))"              !Group "DATA_OUT" = ports 1,0
80   OUTPUT @Dft;"GRO DATA_OUT"                            !Select "DATA_OUT"
90   OUTPUT @Dft;"GRO:MODE STIM"                           !Set group mode to STIMulus
100  OUTPUT @Dft;"STIM:PATT:SEQ:PART 0,1,2,4,8,16,32,64,128"!Output STIMulus pattern
110  OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                     !Use STIMulus clock 0
111  !..... Set up Timing Cycle and Resolution .....
120  OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                        !Delete all previous timing cycles
130  OUTPUT @Dft;"TIM:CYCL:DEF TC_1,750"                   !Timing cycle "TC_1" has 750 subcycles
140  OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,9,TC_1"               !Assign "TC_1" to all sequences
150  OUTPUT @Dft;"TIM:RES 400E-6"                          !Timing resolution = 400 usec
```

(continued on next page)

```
151  !.....Enable Looping and Windows.....
160  OUTPUT @Dft;"DIAG:SEQ:LOOP ON"          !Enable looping for "TEST_1"
170  OUTPUT @Dft;"SEQ:WIND ON"               !Enable window for "TEST_1"
180  FOR I=1 TO 2                            !Execute two RUNs
190    IF I=1 THEN
200      OUTPUT @Dft;"DIAG:SEQ:LOOP:BOUN 2,7"   !Loop boundaries = 2,7 for first RUN
210      OUTPUT @Dft;"SEQ:WIND:BOUN 0,7"        !Window boundaries = 0,7 for first
                                                 RUN
220    ELSE
230      OUTPUT @Dft;"DIAG:SEQ:LOOP:BOUN 0,7"   !Loop boundaries = 0,7 for second RUN
240      OUTPUT @Dft;"SEQ:WIND:BOUN 1,6"        !Window boundaries = 1,6 for second
                                                 RUN
250    END IF
260    OUTPUT @Dft;"RUN"                       !RUN program
270    WAIT 10                                 !Wait 10 seconds
280    OUTPUT @Dft;"STOP"                      !STOP sequence operation
290  NEXT I                                    !Next RUN
300  OUTPUT @Dft;"*RST"                        !Reset instrument
310  END
```

DIAGnostic:SEQuence:LOOP[:STATe]

DIAGnostic:SEQuence:LOOP[:STATe] *1|0|ON|OFF* allows the user to enable or disable a hardware-based looping capability. When activated, the RUN command will cause the hardware to run the currently selected sequence (DIGital:SEQuence:SELect<*seq_name*>) and enter the loop defined by the LOOP:BOUNdary command.

DIAGnostic:SEQuence:LOOP[:STATe]? returns the state of the loop function for the currently selected sequence: enabled (1) or disabled (0).

Parameters

Parameter Name	Parameter Type	Range of Values
1|0|ON|OFF	numeric NR1| discrete	1|0|ON|OFF (ON or OFF can be used instead of 1 or 0). 1 or ON enables looping, 0 or OFF disables looping.

Comments

- **General Conditions**: The state is set to OFF at power-on or after a *RST. TIMing:MARKers cannot be used within the loop. RESPonse:COMPare groups are not able to track compare errors correctly.
- **TIM:MARK and RESP:COMP:** The PAUSe, STEP, and CONTinue commands will work correctly while a loop is active. However, TIMing:MARKers cannot be used within the loop and GROups with RESPonse:COMPare turned on will not be able to track compare errors correctly.
- **Only STOP/PAUSE/ *RST Stop Looping**: Once a loop is RUNning, only the STOP, PAUSE, or *RST commands will STOP the Model D20.

Example Program

See "*Example: Looping a Sequence*".

DIAGnostic: SEQuence: MEMory

DIAGnostic:SEQuence:MEMory commands make use of special, high-speed GPIB transfers to load and read attribute and pattern data directly to and from the instrument hardware. Grouping and Sequence mechanisms cannot be used, so each port must be filled individually.

These commands perform raw loads (writes) and dumps (reads) of sequence memory for the port you specify in the command (or loads of sequence memory for the timing module), without regard to the group or sequence boundaries established by the DIGital:GROup or DIGital:SEQuence subsystems.

When you set up the Model D20, you can use SEQ:SEL and STIM:PATT:SEQ:PART or STIM:PATT:SEQ[:FULL]. However, if you want to quickly load pattern data for a large number of sequences into a **single** Pattern I/O Module port, you can use the DIAGnostic:SEQuence:MEMory command.

NOTE

The DIAG:SEQ:MEM command can be used to load timing tags into memory when the command is addressed to the timing module. However, this is not recommended since there is only marginal speed advantage to using DIAG commands rather than TIM:CYCL:SEQ.

Subsystem Syntax

DIAGnostic:SEQuence:MEMory Subsystem	Description
:SEQuence	
:MEMory	
:ATTRibute <module_#>,<port>,<seq_addr>,<block>	Loads attribute field for sel sequence
:ATTRibute? <module_#>,<port>,<seq_addr>,<count>	Queries attribute field
[:COMBined] <module_#>,<port>,<seq_addr>,<block>	Loads attribute field and data field
[:COMBined]? <module_#>,<port>,<seq_addr>,<count>	Queries attribute field and data field
:DATA <module_#>,<port>,<seq_addr>,<block>	Loads data field for sel sequence
:DATA? <module_#>,<port>,<seq_addr>,<count>	Queries data field

DIAG:SEQ:MEM Command Overview

As shown in Figure 5-3, the sequence for each vector loaded into memory is divided into two fields: an **attribute field** (bits 8 through 15) and a **data field** (bits 0 through 7). DIAG:SEQ:MEM:ATTR/ATTR? loads and dumps to the attribute field, DIAG:SEQ:MEM: DATA/DATA? loads and dumps to the data field, and DIAG:SEQ: MEM [:COMB]/[:COMB]? loads and dumps to both fields.

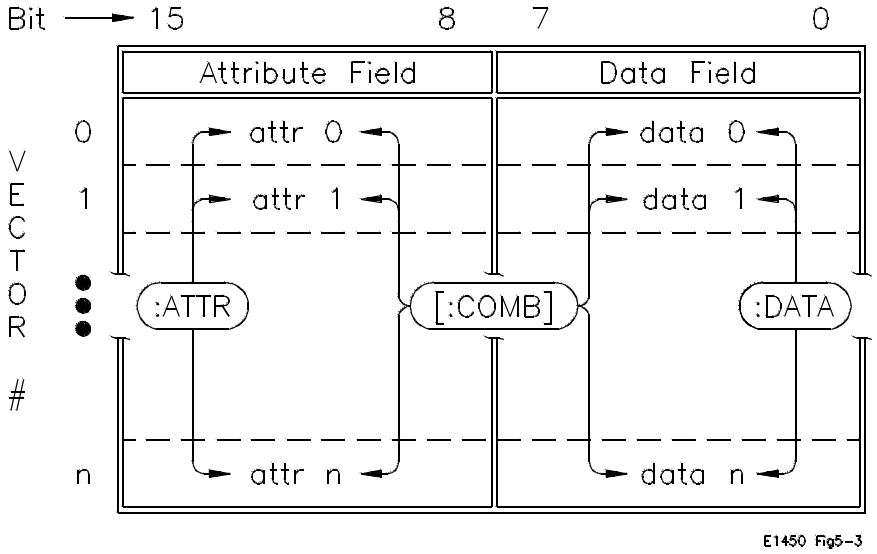


Figure 5-3. Attribute and Data Fields

Timing Module Fields

Figure 5-4 shows the Timing Module attribute and data field definitions and associated (decimal) bit values. Note that bits 8, 9, 12, and 13 are a "don't care" when written, but always return a "1" when read. When the DIAG:SEQ:MEM:ATTR command is used, the attribute field bit values are 1 (bit 8) through 128 (bit 15). However, when the DIAG:SEQ:MEM[:COMB] command is used, the attribute field bit values are 256 (bit 8) through 32768 (bit 15).

Pattern I/O Module Fields

Figure 5-5 shows the Pattern I/O Modules attribute and data field definitions and associated (decimal) bit values. Note that bits 8, 9, 14, and 15 are a "don't care" when written, but always return a "1" when read. When the DIAG:SEQ:MEM:ATTR command is used, the attribute field bit values are 1 (bit 8) through 128 (bit 15). However, when the DIAG:SEQ:MEM[:COMB] command is used, the attribute field bit values are 256 (bit 8) through 32768 (bit 15).

Definition	BKPT	TRIG	X	X	MARK	EOS	X	X

Readback = 1

BKPT: 1 = a breakpoint will occur before this cycle
TRIG: 1 = the trigger will be armed before this cycle
MARK: 1 = a marker pulse will be generated in this cycle
EOS: 1 = this cycle is the end of the sequence

Timing Module – Data Fields

Bit Value	128	64	32	16	8	4	2	1
Bit #	7	6	5	4	3	2	1	0
Definition	TIMING CYCLE TAG							

TIMING CYCLE TAG: The first subcycle of this cycle is located at the timing generator memory location that has an address equal to four times this value.

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Figure 5-4. Timing Module Attribute/Data Fields

Pattern I/O Modules – Attribute Fields

Bit Value [:COMB] Bit Value :ATTR	32768 128	16384 64	8192 32	4096 16	2048 8	1024 4	512 2	256 1
Bit #	15	14	13	12	11	10	9	8
Definition	X	X	COMP	TRIS	BRA	EOS	X	X

Readback = 1

COMP: Enables (1) or disables (0) the compare test
TRIS: Drives (0) or tristates (1) the stimulus stage
BRA: Branch. If set (1) causes jump to branch destination
EOS: End of Sequence. If set (1), causes sequencer to stop

Pattern I/O Modules – Data Fields

Bit Value	128	64	32	16	8	4	2	1
Bit #	7	6	5	4	3	2	1	0
Definition	PATTERN DATA							

E1450 Fig5-5

Figure 5-5. Pattern I/O Modules Attribute/Data Fields

DIAGnostic:SEQuence:MEMory:ATTRibute

DIAGnostic:SEQuence:MEMory:ATTRibute <*module_#*>,<*port*>, <*seq_addr*>,<*block*> performs a direct load of the attribute field for the memory of the given port. Sequence memory begins loading at the memory location specified by the parameter <*seq_addr*>. The attribute field consists of the upper (most-significant) eight bits of the memory word.

DIAGnostic:SEQuence:MEMory:ATTRibute?<*module_#*>,<*port*>, <*seq_addr*>,<*count*> returns the attribute field for the given port's sequence memory. The number of memory locations specified by the <*count*> parameter is returned, beginning with <*seq_addr*>.

Parameters

Parameter Name	Parameter Type	Range of Values
<module_#>	numeric NRf	0 to number of last module (must be 0 for Timing Module)
<port>	numeric NR1	0, 1, 2, or 3 (must be 0 for Timing Module)
<seq_addr>	numeric NRf	0 to 65535
<count>	numeric NRf	1 to number of memory locations to be read
<block>	Definite or indefinite length block	

Comments

- **General Information:** DIAG:SEQ:MEM:ATTR requires one byte per memory location. The <*port*> parameter must be 0 for the Timing Module. <block> can be in definite or indefinite length format. The DIAG:SEQ:MEM:ATTR? response is definite-length arbitrary block data, with one byte per memory location.
- **Timing Module Attribute Field:** Figure 5-4 shows the attribute field for the Timing Module memory. Bits 8, 9, 12, and 13 are a "don't care" when written and return a "1" when read.
- **Pattern I/O Port Attribute Field:** Figure 5-5 shows the attribute field for each sequence addressed to a port memory. Bits 8, 9, 14, and 15 are a "don't care" when written and return a "1" when read.

Example Program

See "DIAGnostic:SEQuence:MEMory[:COMBined]" command.

DIAGnostic:SEQuence:MEMory[:COMBined]

DIAGnostic:SEQuence:MEMory[:COMBined]<*module_#*>, <*port*>, <*seq_addr*>,<*block*> performs a direct load of both the attribute field and the data field for the selected sequence memory. Sequence memory begins loading the <*block*> of attribute/pattern data at <*seq_addr*>.

DIAGnostic:SEQuence:MEMory[:COMBined]? <*module_#*>, <*port*>, <*seq_addr*>, <*count*> returns both fields for the selected sequence memory. The number of memory locations returned is set by <*count*>. The dump begins at the memory location specified by the <*seq_addr*> parameter.

Parameters

Parameter Name	Parameter Type	Range of Values
<module_#>	numeric NRf	0 to number of last module (must be 0 for Timing Module)
<port>	numeric NR1	0, 1, 2, or 3 (must be 0 for Timing Module)
<seq_addr>	numeric NRf	0 to 65535
<count>	numeric NRf	1 to number of memory locations to be read
<block>	Definite or indefinite length block	

Comments

- **General Information**: DIAG:SEQ:MEM [:COMB] requires two bytes per memory location: attribute byte first, then the data byte. The <*port*> parameter must be 0 for the Timing Module. Output can be in definite or indefinite length blocks. The DIAG:SEQ:MEM[:COMB]? response is in definite length format, with two bytes per memory location**.**
- **Timing Module Attribute Field:** Figure 5-4 shows the attribute and data fields for the Timing Module memory. Bits 8, 9, 12, and 13 are a "don't care" when written and return a "1" when read. All other bits return the last values written when read (assuming no AUTO INCR).

  If bit 5 of the Status/Control Register #1 (06_H) is set, bit 15 cannot be written to. If bit 4 of the Status/Control Register #1 (06_H) is set, bit 8 cannot be written to.

- **Pattern I/O Port Attribute/Data Fields:** Figure 5-5 shows the attribute and data fields for each vector of a sequence addressed to a port memory. Bits 8, 9, 14, and 15 are a "don't care" when written and return a "1" when read.

Example Program

This program uses DIAG:SEQ:MEM[:COMB]/[:COMB]? to enter and read a block of attribute and data pattern data for sequence "TEST_1" that has 8 vectors. The inputs are to Pattern I/O Module 1, port 0. Before running this program, connect ports 0 and 1 of the Light Board to a Pattern I/O Module in slot 1, and set SW2 to OPEN.

When the sequence is RUN, the Light Board port 0 lights should light for patterns 1, 2, 3, 4 and 5 and then remain ON for pattern 6. To run the following program:

- Insert *Model D20 Service Programs Disk* in disk drive
- Load DIAGnostic programs with LOAD "DIAG_CMD"
- Press RUN
- Select "*Example: Attribute/Data Fields*"

```
1     ! Example: Attribute/Data Fields
2     !
3     !------------------------------------ Define attribute/data fields ---------------------------------
10    CLEAR SCREEN
20    DISP CHR$(129)                                  !Inverse video on display
30    INTEGER Out_dat(0:7),In_dat(0:7)                !INTEGER input and output paths
40    ASSIGN @Out_buf TO BUFFER [1000]                !Assign outut path to buffer
50    ASSIGN @In_buf TO BUFFER [1000]                 !Assign input path to buffer
60    ASSIGN @Dft TO 70917                            !Assign path to Model D20
70    DATA 0,8193,2,8195,4,8197,1030,7                !Enter attribute/data patterns
80    READ Out_dat(*)                                 !Read patterns
81    ! -------------------------Clear attribute/data fields ------------------------------------------------------
90    PRINT "Clearing attribute and data fields ....."
100   OUTPUT @Dft;"TEST?"                             !Clear attribute/data fields
110   ENTER @Dft;Test_end                             !End TEST?
111   !---------------------------------- RUN sequence ------------------------------------------------------------
120   OUTPUT @Dft;"*RST"                              !Set instrument to known state
130   OUTPUT @Dft;"SEQ:DEL:ALL"                       !Delete all previous sequences
140   OUTPUT @Dft;"SEQ:DEF TEST_1,8"                  !Sequence "TEST_1" has 8 vectors
150   OUTPUT @Dft;"SEQ TEST_1"                        !Select "TEST_1"
```

(continued on next page)

```
160  OUTPUT @Dft;"GRO:DEL:ALL"                          !Delete all previous pin groups
170  OUTPUT @Dft;"GRO:DEF OUT,(@1(0))"                  !Pin group "OUT" = module 1, port 0
180  OUTPUT @Dft;"GRO OUT"                              !Select pin group "OUT"
190  OUTPUT @Dft;"GRO:MODE STIM"                        !Set goupt to STIMulus mode
200  OUTPUT @Dft;"STIM:CLOC:SOUR INT0"                  !Select internal clock 0
210  OUTPUT @Dft;"TIM:CYCL:DEL:ALL"                     !Delete all previous timing cycles
220  OUTPUT @Dft;"TIM:CYCL:DEF TC_1,750"                !Timing cycle "TC_1" has 750 subcycles
230  OUTPUT @Dft;"TIM:CYCL:SEQ:REP 0,8,TC_1"            !Repeat timing cycle for all 8 vectors
240  OUTPUT @Dft;"TIM:RES 400E-6"                       !Resolution = 400 usec
250  OUTPUT @Dft;"DIAG:SEQ:MEM 1,0,0, ";                !Output fields to module 1, port 0,
                                                        seq_addr 0
260  CALL Send_patt(@Dft,@Out_buf,Out_dat(*))           !Call subprogram to output block data
270  CLEAR SCREEN
280  DISP " Press Continue to RUN this sequence "
290  PAUSE
300  CLEAR SCREEN
310  OUTPUT @Dft;"RUN"                                  !RUN sequence
320  CALL Read_patt(@Dft,@In_buf,In_dat(*),Out_dat(*))  !Call subprogram to read data
330  END
331  !---------- Send attribute/pattern fields to port 0 ----------
340  SUB Send_patt(@Dft,@Out_buf,INTEGER Out_dat(*))
350    OUTPUT @Out_buf USING "#,Y";Out_dat(*)           !Output data in word (two-byte) format
360    OUTPUT @Dft;"#0";                                !Indefinite length block data
370    TRANSFER @Out_buf TO @Dft;WAIT                   !Transfer data to buffer
380    OUTPUT @Dft USING "#,B";10,END                   !Output data to module 1, port 0
390  SUBEND
400  !---------- Read attribute/pattern fields in port 0 ----------
410  SUB Read_patt(@Dft,@In_buf,INTEGER In_dat(*),INTEGER Out_dat(*))
420    INTEGER Blk_size,Digit_count,Prefix,Digit
430    REPEAT
440      OUTPUT @Dft;"STAT:OPER:COND?"                  !Monitor Operation Status Register
                                                        contents
450      ENTER @Dft;A                                   !Enter contents
460    UNTIL BIT(A,8)=1                                 !Continue when bit 8 (instrument
                                                        STOPped) = 1
470    OUTPUT @Dft;"DIAG:SEQ:MEM? 1,0,0,8"              !Query module 1, port 0 memory
480    ENTER @Dft USING "#,B,B";Prefix,Digit_count       !Enter data
490    Prefix$=CHR$(Prefix)                             !Convert prefis to string
500    Digit_count=Digit_count-NUM("0")                 !Initial digit_count
510    Blk_size=0
```

(continued on next page)

```
520    FOR I=1 TO Digit_count                                  !Begin loop
530      ENTER @Dft USING "#,B";Digit                          !Enter digit value
540      Digit=Digit-NUM("0")                                  !Set initial digit value
550      Blk_size=Blk_size*10                                  !Define block size
560      Blk_size=Blk_size+Digit                               !Change block size
570    NEXT I                                                  !Next count
580    TRANSFER @Dft TO @In_buf;COUNT Blk_size,WAIT            !Transfer data to buffer
590    ENTER @Dft USING "#,B";Digit                            !Enter digit value
600    ENTER @In_buf USING "#,Y";In_dat(*)                     !Enter data from buffer
610    DISP " Press Continue to display attribute and data patterns "
620    PAUSE
630    PRINT
640    PRINT "Vector     Attr/Data Pattern sent          Attr/Data Pattern read"
650    PRINT
660    PRINT "      Decimal  Attr Bits  Data Bits     Decimal  Attr Bits  Data Bits"
670    PRINT "                  [15---8]    [7---0]                  [15---8]    [7---0]"
680    PRINT
690    FOR I=0 TO 7
700      A$(I)=IVAL$(Out_dat(I),2)
710      B$(I)=IVAL$(In_dat(I),2)
720 Format:IMAGE 2X,D,4X,S5D,3X,8A,3X,8A,6X,S5D,3X,8A,3X,8A
730      PRINT USING Format;I,Out_dat(I),A$(I)[1,8],A$(I)[9,16],In_dat(I),B$(I)[1,8],B $(I)[9,16]
740    NEXT I
750    DISP ""
760    OUTPUT @Dft;"*RST"
770  SUBEND
```

Typical Results

Three displays follow for this program. In each display, the decimal values sent with DIAG:SEQ:MEM [:COMB] set the bit pattern for each vector. The first display shows the results when DIAG:SEQ: MEM [:COMB]? is used, the second display shows the results when DIAG:SEQ: MEM:ATTR? is used, and the third display shows the results when DIAG:SEQ: MEM:DATA? is used.

For example, since the command is sent to a Pattern I/O Module, "8193" enables the comparison test (bit 13 set with "8192") and sends data pattern 00000001 (bit 1 set with "1"). The overall result is set by entering the sum for the attribute and data field entries ("8193" = "8192" + "1").

Since the Pattern I/O Modules always return "1" for bits 8, 9, 14, and 15, "-15616" is added to the decimal value sent to the module. For example, for vector 1 "-15616" is added to "+8193" for a returned value of "-7423".

Display Using [:COMB] and [:COMB]?

Vector	Attr/Data Pattern sent			Attr/Data Pattern read		
	Decimal	Attr Bits [15---8]	Data Bits [7---0]	Decimal	Attr Bits [15---8]	Data Bits [7---0]
0	+0	00000000	00000000	-15616	11000011	00000000
1	+8193	00100000	00000001	-7423	11100011	00000001
2	+2	00000000	00000010	-15614	11000011	00000010
3	+8195	00100000	00000011	-7421	11100011	00000011
4	+4	00000000	00000100	-15612	11000011	00000100
5	+8197	00100000	00000101	-7419	11100011	00000101
6	+1030	00000100	00000110	-14586	11000111	00000110
7	+7	00000000	00000111	-15609	11000011	00000111

Display Using [:COMB] and :ATTR?

This display shows typical results when DIAG:SEQ:MEM[:COMB] and DIAG:SEQ:MEM:ATTR? are used. To get this display, change the following program lines to the form shown and reRUN the program.

```
    470  OUTPUT @Dft;"DIAG:SEQ:MEM:ATTR? 1,0,0,8"
    600  ENTER @In_buf USING "#,B";In_dat(*)
    730  PRINT USING
Format;I,Out_dat(I),A$(I)[1,8],A$(I)[9,16],In_dat(I),B$(I)[9,16]
```

Vector	Attr/Data Pattern sent			Attr/Data Pattern read		
	Decimal	Attr Bits [15---8]	Data Bits [7---0]	Decimal	Attr Bits [15---8]	Data Bits [7---0]
0	+0	00000000	00000000	+195	11000011	
1	+8193	00100000	00000001	+227	11100011	
2	+2	00000000	00000010	+195	11000011	
3	+8195	00100000	00000011	+227	11100011	
4	+4	00000000	00000100	+195	11000011	
5	+8197	00100000	00000101	+227	11100011	
6	+1030	00000100	00000110	+199	11000111	
7	+7	00000000	00000111	+195	11000011	

Display Using [:COMB] and :DATA?

This display shows typical results when DIAG:SEQ:MEM[:COMB] and DIAG:SEQ:MEM:DATA? are used. To get this display, change the following program lines to the form shown, and reRUN the program.

```
470  OUTPUT @Dft;"DIAG:SEQ:MEM:DATA? 1,0,0,8"
600  ENTER @In_buf USING "#,B";In_dat(*)
720 Format:IMAGE 2X,D,4X,S5D,3X,8A,3X,8A,6X,S5D,15X,8A
730  PRINT       USING Format;I,Out_dat(I),A$(I)[1,8],A$(I)[9,16],
In_dat(I),B$(I)[9,16]
```

Vector	Attr/Data Pattern sent			Attr/Data Pattern read		
	Decimal	Attr Bits [15---8]	Data Bits [7---0]	Decimal	Attr Bits [15---8]	Data Bits [7---0]
0	+0	00000000	00000000	+0		00000000
1	+8193	00100000	00000001	+1		00000001
2	+2	00000000	00000010	+2		00000010
3	+8195	00100000	00000011	+3		00000011
4	+4	00000000	00000100	+4		00000100
5	+8197	00100000	00000101	+5		00000101
6	+1030	00000100	00000110	+6		00000110
7	+7	00000000	00000111	+7		00000111

DIAGnostic:SEQuence:MEMory:DATA

Description

DIAGnostic:SEQuence:MEMory:DATA <*module_#*>,<*port*>, <*mem_addr*>,<*block*> loads the pattern data field for the selected sequence memory. Loading begins at the memory location specified by the <*seq_addr*> parameter.

DIAGnostic:SEQuence:MEMory:DATA? <*module_#*>,<*port*>, <*mem_addr*>,<*count*> returns the contents of the data field for the selected sequence memory. <*count*> locations are returned beginning at <*seq_addr*>.

Parameters

Parameter Name	Parameter Type	Range of Values
<module_#>	numeric NRf	0 to number of last module (must be 0 for Timing Module)
<port>	numeric NR1	0, 1, 2, or 3 (must be 0 for Timing Module)
<seq_addr>	numeric NRf	Memory (sequence) addresses
<count>	numeric NRf	1 to number of memory locations to be read
<block>	Definite or indefinite length block	

Comments

- **General Information:** DIAG:SEQ:MEM:DATA requires one byte per memory location. The <*port*> parameter must be 0 for the Timing Module. <block> can be in definite or indefinite length format. The DIAG:SEQ:MEM:DATA? response is definite-length arbitrary block data, with one byte per memory location.
- **Timing Module Data Field:** Figure 5-4 shows the data field for the Timing Module.
- **Pattern I/O Port Data Field:** Figure 5-5 shows the data field for each vector of a sequence addressed to a port memory.

Example Program

See "DIAGnostic:SEQuence:MEMory[:COMBined]" command.

DIAGnostic: SYSTem:HEALth

The **DIAGnostic:SYSTem:HEALth** subsystem controls the hardware status (health) monitoring capability of the Model D20. A "healthy" port means that it is functional with respect to the other ports of the instrument.

For example, in a Model D20 where some ports have pods attached, but other ports do not, the ports without pods are considered "sick" (i.e., they cannot correctly compensate their clocks to match ports that have pods). Also, any Model D20 port or timing module with a detected hardware defect will be identified as "sick".

Subsystem Syntax

DIAGnostic:SYSTem:HEALth Subsystem	Description
DIAGnostic :SYSTem :HEALth :CHECk 1|0|ON|OFF :CHECk? [:STATus]?	 Enables/disables health check Queries health check state Returns health of all hardware

DIAGnostic:SYSTem:HEALth:CHECk

Description

DIAGnostic:SYSTem:HEALth:CHECk *1|0|ON|OFF* enables or disables the "health" check of ports in a digital group.

DIAGnostic:SYSTem:HEALth:CHECk? returns the current state of the HEALth:CHECk as an NR1 numeric response: (1) = enabled and (0) = disabled.

Parameters

Parameter Name	Parameter Type	Range of Values
1|0|ON|OFF	numeric NR1| discrete	1|0|ON|OFF (ON or OFF can be used instead of 1 or 0). 1 or ON enables health evaluation. 0 or OFF disables health evaluation.

Comments

- The DIGital:GROup:DEFine command normally requires all ports in a port list to be "healthy" when forming a group. However, the DIAGnostic:SYSTem:HEALth:CHECk command can direct the DIGital:GROup:DEFine command to ignore the "health" of ports when forming a group.

- Setting DIAG:SYST:HEAL:CHEC to 0 or OFF causes port "health" to be ignored and you can use commands such as STIMulus:PATTern:VALue <*pattern_value*> to output a pattern to a group **even though its ports have failed self-test.** At power-on and after *RST, this parameter will be set to 1 (ON).

DIAGnostic:SYSTem:HEALth[:STATus]?

Description

DIAGnostic:SYSTem:HEALth[:STATus]? returns information on the current "health" of the instrument as a list of quoted strings. There is one string for each module in the instrument. Each string contains six decimal numeric values of the form <*module_#*>,<*device_id*>, <*health*> ,<*health*>,<*health*>,<*health*>,<*health*>

<device_id> The decimal numeric value of the module code field in the module's Device Type VXI register:

Module Name	device identification
E1451A Pattern I/O Module	337
E1450A Timing Module	338
E1452A Terminating Pattern I/O Module	339

<health> Fields

Pattern I/O Modules have one health field for each port: "<*health*>,<*health*>,<*health*>,<*health*>". The Timing Module uses only the first health field, and the last three are zero ("<*health*>,0,0,0"). A <*health*> field response of "0" indicates no hardware problems are identified. A non-zero <*health*> field response indicates a problem as shown in the following table:

Bit #	Decimal Value	Description
0	1	Module calibration RAM checksum failed.
1	2	No pod attached when others in the instrument have pods. Or, pod type does not match type of first pod found.
2	4	Pod calibration RAM has failed.
3	8	Insufficient range in delay device to calibrate.
4	16	Self-test failure.

Typical Return

For a Timing Module and one Terminating Pattern I/O Module installed, a typical return for the DIAG:SYST:HEAL[:STAT]? command might be "0,338,17,0,0,0","1,339,0,0,0,0".

For this return "0,338,17,0,0,0" indicates the Timing Module (*module_#* 0 and *device_id* 338) has failed self-test (decimal value 16) and its module calibration RAM checksum has failed (decimal value 1). The decimal value response in the first <*health*> field = 16 + 1 = 17.

Note that the last three <*health*> fields are always "0" for the Timing Module. The return for the Pattern I/O Module (*module_#* 1 and *device_id* 339) indicates all ports "healthy" since "0,0,0,0" is returned.

DIAGnostic: TIMing:VALid?

DIAGnostic:TIMing:VALid? [<*start_vector*>] returns any problems found after analyzing the currently selected TIMing:CYCLe:SEQuence. Analysis begins at the vector specified by <*start_vector*> and proceeds to the end of the sequence.

Subsystem Syntax

DIAGnostic:TIMing:VALid? Subsystem	Description
DIAGnostic :TIMing :VALid?[<start_vector>]	Validates selected TIM:CYCL:SEQ

DIAGnostic:TIMing:VALid?

Description

DIAGnostic:TIMing:VALid? [<*start_vector*>] returns any problems found after analyzing the currently selected TIMing:CYCLe:SEQuence. Analysis begins at the vector specified by <*start_vector*> and proceeds to the end of the sequence.

Four values are returned in NR1 numeric format. The response string is: "<*first value*>,<*second value*>,<*third value*>,<*fourth value*>", where the description of each value is:

Value	Description of value meaning
first value	Count of invalid tags that do not point to a currently defined timing cycle.
second value	Count of cycles with a non-producible pulse in their Control Output waveforms.
third value	Count of cycles with pattern clock compatibility problems, that is, the combination of the cycle with its preceding cycle produces an illegal clock interval.
fourth value	The vector number at which the first defect was detected.

Comments

- See *Chapter 3 - Special Topics*, in the *Model D20 Task and Command Reference* manual for information on adjacent timing cycles and using clock pulses in the last two subcycles.
- The effects of EIReady points on the validity of Control Output waveforms and pattern clock compatibility are NOT considered. If the EIReady function is used, extra checking by the user is required.

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